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LOW-κ MATERIALS: ETCH RESIDUE REMOVAL

Characterizing Etch Residue Removal For Batch Processing of Spin-On Low-κ Dielectric Materials

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ABSTRACT

Popular spin-on variety low-κ dielectric materials, including SiLK [1-2] and methylsilsesquioxane (MSQ), are being integrated into BEOL semiconductor wafer processing. Post-etch residue removal from low-κ/copper structures requires selective dissolution of the organometallic without effect to the material stack or the base metal. The chemistry of choice must overcome process deviation across the wafer, where variations in the plasma chemistry cause an increase in residue at the wafer edge.

At times, this deviation may account for as much as a five-fold increase in the amount of etch residue as compared to the wafer center. Successful etch residue removal requires high-strength chemistries to leach impregnated metal and expose organic moieties where they may be dissolved and rinsed away. Production worthiness of the chemistry must provide complete solubility such that conventional batch processing tools may capture, filter, and recirculate the stripper back onto the wafer. General Chemical Corporation has developed a substrate-safe stripper, GenSolve 670, to meet this requirement. When used at moderate temperatures in a batch-style spray tool, etch residue is dissolved in minutes. A complete cycle time of 30 minutes is possible, providing a throughput near 200 wafers/hour depending upon size of the wafers. Bath life studies suggest material performance is preserved over several cycles, offering significant loading levels and reduced costs. Simple rinse methods remove potentially absorbed stripper as demonstrated by selective FTIR methods.

Surface analysis of copper metal suggests a 3 to 5 monolayer conversion from Cu(II) to Cu(I), providing necessary protection from native oxide growth. Additional processing data will be provided on GenSolve 670 used with SiLK and MSQ low-κ integrated devices.

In most batch spray tools, the stripper will be collected and returned to the heated reservoir where it is brought back up to operating temperature in preparation for the next group of wafers.

INTRODUCTION

The removal of etch residue from organic spin-on dielectrics (SODs) is commonly done with special chemistries in an automated tool. A successful cleaning process involves overcoming many challenges. These include the rapid dissolution of metal-bearing resist residue, little or no attack to the substrate or materials in the stack, reliable rinsing without redeposition, and the minimization of variation across the wafer. By proper characterization of the etch residue and its removal, a good understanding of the chemistry and how it may be controlled in a tool is achieved.

As the semiconductor industry continues to push for better interconnect efficiency, more pressure is leveraged on the implementation of smaller geometries composed of high conductivity metals such as copper with an interlayer dielectric (ILD) exhibiting an ultra low dielectric constant (low κ) value. These multilayer metal wiring schemes are processed in many ways to include the copper damascene method with the dielectric applied through chemical vapor deposition (CVD) or with a SOD [3]. Although CVD dielectrics have many benefits, the focus of this paper is on SODs to include the SiLK and MSQ varieties.

SiLK and MSQ are organic polymers based upon a polyphenylene or a siloxane molecular species, respectively. When used as an ILD, the polymer is commonly spun onto a hard etch stop such as SiC and capped with SiO_2 [4]. This "sandwich" of dissimilar materials provides a framework which

helps to maintain rigidity and lower thermal-induced dimensional change (see Figure 1). When patterning, the etch chemistry and process must be adjusted to accommodate the range of materials in the ILD sandwich. Changes in etch chemistry and conditions will reflect irregular residue formation and ultimately contribute to variability in residue across the wafer. When this occurs, residue may be heavy at the wafer edge. More etch residue will typically extend out the cleaning process which may sacrifice selectivity, increase absorption into the ILD and reduce throughput.

DENSE AND POROUS SILK STACK

Two forms of SiLK SOD were evaluated. Wafers were prepared by International SEMATECH in conjunction with Dow Chemical [5]. Similar reticles were utilized for both wafer lots; however, the nodes were 0.25 micron and 0.175 micron, respectively, for dense and porous. The stack is similar for each as defined in Figure 1.

MSQ STACK

The MSQ stack test specimens are part of a damascene structure consisting of 1000 Å SiCO (hard mask), 4000 Å porous MSQ, and 1000 Å SiCN (barrier layer) opened to copper metal substrate. This "sandwich" is similar to that described earlier and parallels the stack appearance depicted in Figure 1. The wafers were prepared by International SEMATECH using 0.25 micron geometry.

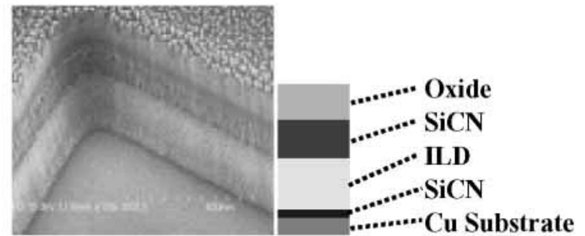
ETCH RESIDUE CHARACTERIZATION

Etch residue on the SiLK wafers was observed on the wall extending to the substrate. The wall definition is lost and appears to be smooth, suggesting a surface coating. Etch residue on the dense SiLK wafer was heavy at the edge as compared to the center, indicating that optimization of the etch process was needed. The porous wafers were observed to have more residue on the substrate, yet have a consistent residue content on the area side wall throughout the wafer. SEM photos of residue on dense and porous SiLK wafers are presented in Figure 2.

An attempt was made to acquire composition analysis of etch residue on dense SiLK by grazing angle energy dispersive X-ray spectroscopy (EDS). Three spectra were taken of an area

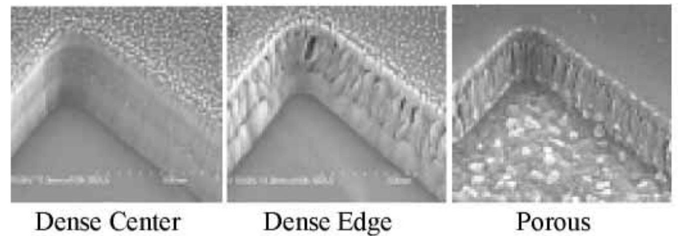
The chemistry of choice must overcome process deviation across the wafer, where variations in the plasma chemistry cause an increase in residue at the wafer edge.

FIGURE 1



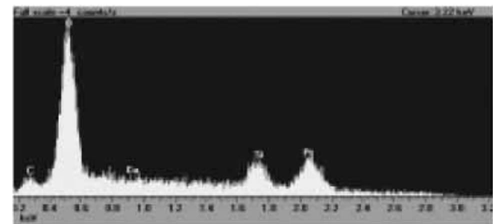
Description of the "sandwiched" SiLK ILD stack.

FIGURE 2

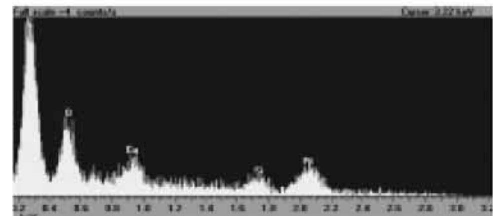


Post-etch residue on SiLK ILD dense center and edge (left and center) and porous (right) stack.

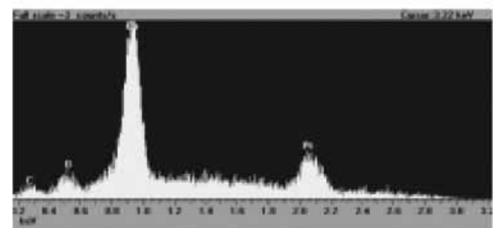
FIGURE 3



A EDS of top area of side wall. Note oxide peak.



B EDS of middle area of side wall. Note carbon peak.



C EDS of bottom area of side wall. Note copper peak.

EDS of dense SiLK ILD at specified locations: 3a) top area, 3b) middle, and 3c) bottom.

along the side wall traveling from top to bottom. Figure 3 includes the spectra of the noted areas tested: a) top (oxide SiO_2), b) middle (ILD polymer), and c) bottom (substrate copper).

The EDS data in Figure 3 suggests not just the elemental confirmation of the stack noted in Figure 1, but also the presence of copper in the residue (middle) portion of the wall. The presence of copper in the residue is common and represents the backsplash from the substrate when used as the etch-stop.

A review of the etch residue on the MSQ wafers indicates that the material is different in amount and appearance. Namely, residue was noted in the top of the via and at the substrate. Figure 4 depicts the residue noted from MSQ etch processing.

PROCESS REMOVAL CHEMISTRY

Since copper is the substrate for the test series containing SiLK and MSQ, there is expected to be a certain amount of copper-bearing polymer residue along the wall. Removal requires a chemistry that will offer complexing to an extent that triggers selective dissolution of that material on the wall without changing the integrity of the bulk substrate metal.

The chemistry used in this cleaning application, GenSolve 670, is based upon the use of a high molecular weight quaternary ammonium hydroxide with corrosion inhibitors in a sulfoxide solvent-cosolvent medium [6]. This product is designed to have high solubility for polymer substances and trace metal salts while protecting the integrity of bulk (stack) material.

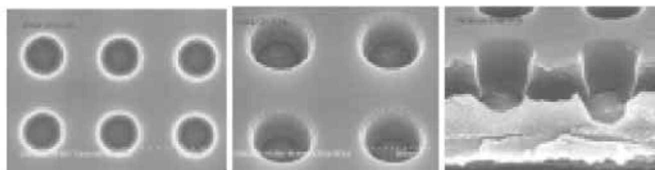
RESIDUE REMOVAL

During reactive ion etching (RIE), part of the resist mask is broken down and incorporated into the plasma and distributed over the entire wafer, causing a preferential redeposition into the vias and troughs. This effect causes anisotropic etching where the residue helps to focus the etch process vertically instead of horizontally. However, the etch process must be optimized such that acceptable resolution occurs here without causing problems down the line during cleaning. Cleaning will normally require formulated chemistries with strong acids or alkalis and corrosion inhibitors [7-11].

Residue removal was carried out using a chemistry from the GenSolve product line. The product has a polar solvent with a high dielectric constant containing a high molecular

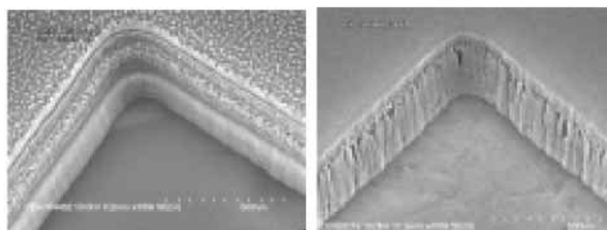
When patterning, the etch chemistry and process must be adjusted to accommodate the range of materials in the interlayer dielectric sandwich.

FIGURE 4



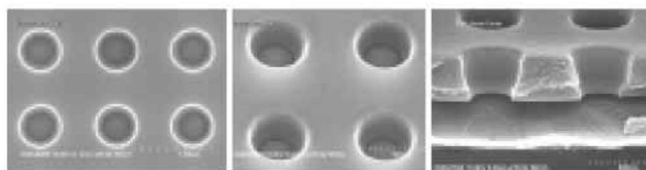
Post-etch residue on MSQ-based ILD vias.

FIGURE 5



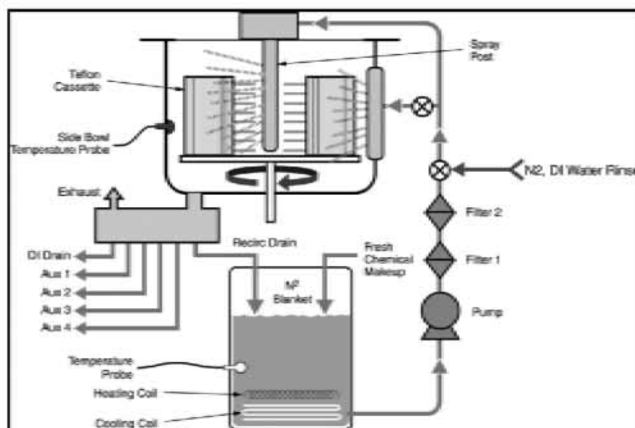
Residue removal from dense (left) and porous (right) SiLK.

FIGURE 6



Residue removal from MSQ ILD vias as compared to Figure 4 (no clean).

FIGURE 7



Schematic diagram of ZETA Surface Conditioning System. Temperature-controlled chemical is dispensed fresh or recirculated from center and side spray posts.

weight quaternary amine and a corrosion inhibitor. The quaternary amine offers excellent dissolution and saponification capacity for carbon containing products while the solvent accepts metal bearing salts. The corrosion inhibitor protects the substrate copper to offer selectivity. Results of the residue removal are shown in Figures 5 and 6 for SiLK and MSQ, respectively. The irregular sidewall appearance of the porous sample is believed to be due to non-optimized etch conditions.

RESIDUE REMOVAL IN AUTOMATED BATCH SPRAY TOOL

Residue removal for BEOL applications requires automated tools to be versatile in terms of the chemical compatibility of the materials of construction, process temperatures and chemical dispense times. Figure 7 shows a schematic diagram of the spray processor used in this study, the FSI International ZETA Surface Conditioning System. This system is a batch spray processor that utilizes centrifugal force for enhanced particle removal and drying. The process chemistry can be dispensed via center and side spray posts from a fresh or recirculated source, depending on chemical cost and dispense time.

Bath lifetime is often critical in minimizing the cost-of-ownership. In addition, BEOL chemistries are often sensitive to oxidation at operating temperatures. Therefore, the system described herein utilizes a nitrogen atmosphere for both the process chamber and chemical storage tanks to minimize chemical degradation. Chemical rinsing is often critical to reduce metallic corrosion which may occur if removal chemistries remain on the wafer during exposure to ambient conditions. The rinsing system shown in Figure 7 is designed so that the center spray post rinses the wafers while the side spray posts are primarily designed to rinse the wafer cassette and rotating turntable. In addition, the rotating turntable is programmable within the process recipe to rotate clockwise or counter-clockwise to eliminate any "shadowing" which can occur if obstacles are present between the chemical stream and wafer.

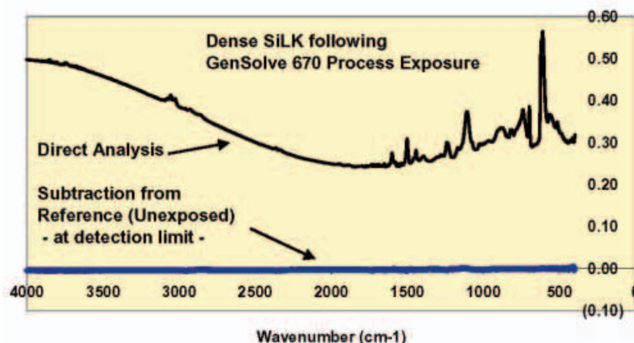
Finally, the process temperature is very important in controlling film loss and maintaining a high selectivity between the residue and substrate. In general, film loss increases and selectivity decreases as the temperature is increased outside the recommended temperature range. Consequently, the tem-

continued on page 138

By matching a chemistry to a tool design, the performance and throughput of the process can be optimized for a batch approach.

FIGURE 8

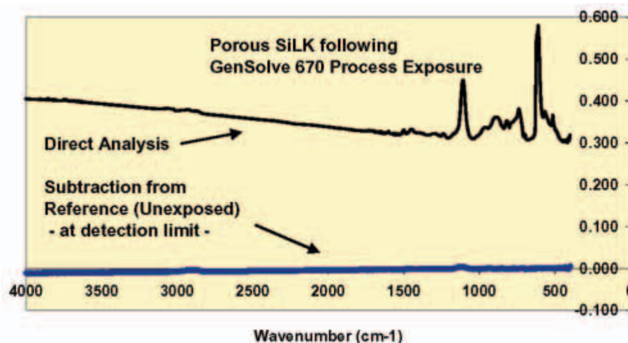
FTIR Analysis of Dense SiLK on Si Wafer Moisture Detection after GenSolve Exposure



FTIR analysis of dense SiLK showing nondetect moisture after exposure to GenSolve 670.

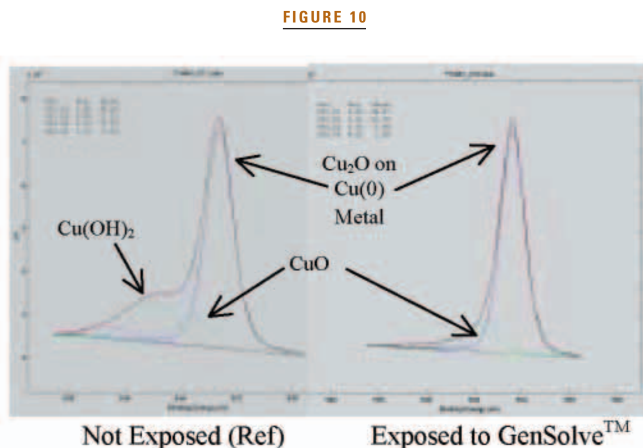
FIGURE 9

FTIR of Porous SiLK Direct on Si Water Moisture Detection after GenSolve Exposure



FTIR analysis of porous SiLK showing nondetect moisture after exposure to GenSolve 670.

FIGURE 10



ESCA/XPS showing Cu 2p spectrum of copper surface for reference and GenSolve exposure. The spectra indicate the conversion of Cu(II) hydroxide to Cu(I) and Cu(0) metal.

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Using a chemistry in a tool that allows simple water rinsing not only reduces environmental health and safety (EH&S) concerns but also simplifies the process.

perature is monitored both at the chemical heater and on the side bowl of the process chamber to accurately control heating and on-wafer chemical temperature. The chemical temperature and flow can be monitored and compensated using a reaction rate algorithm to accurately control film loss within + 2 percent (1σ).

RINSING AND DESORPTION FROM THE ILD

Successful residue removal is not complete without proper attention to rinsing. Since the trend in ILD definition is towards the use of porous materials, it stands to reason that rinsing must effectively penetrate, mix with the stripper and produce sufficient removal with satisfactory drying. Depending upon the ILD in use, the chemistry, and whether the rinse involves water or IPA, a high temperature bake (i.e. >100°C) may be necessary to drive off any residual solvent or moisture in the pores.

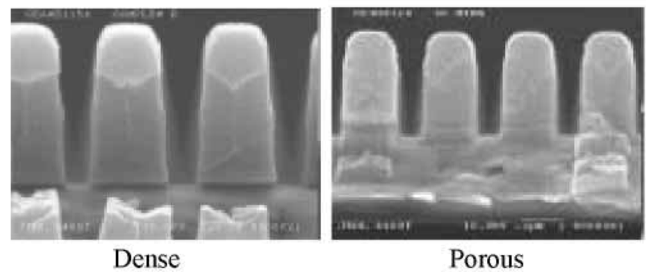
GenSolve 670 is completely polar and infinitely miscible with water or IPA. It is not necessary to use a high temperature bake step following rinsing. A common test for residual moisture or solvent is Fourier transform infrared (FTIR) spectroscopy. Figures 8 and 9 show the results for FTIR studies on SiLK following exposure and rinsing to include a reference subtraction showing detection limit values for the presence of residue and moisture. Similar data was observed for the MSQ ILD wafers as that described in Figures 8 and 9.

SUBSTRATE COMPATIBILITY

The key to selectivity is to ensure that the product is targeted to the metal bearing residue and not the substrate. Although the GenSolve 670 chemistry has been discussed, analysis of the substrate copper may be performed before and after to determine any interactions. Substrates were exposed to GenSolve 670 for 30 minutes at 60° to 70° C, rinsed, and tested. ESCA/XPS is used to analyze the top monolayers of the substrate and determine if damaging effects have occurred. Figure 10 is a spectra of the copper substrate showing that the top layers of metal is present as Cu(I) over Cu(0).

The ESCA/XPS work suggests that the surface of the exposed copper is different than that which is not exposed. The copper surface of the not-exposed (reference) indicates the presence of both the native Cu(II) oxide (adventitious) and hydroxide, whereas the exposed version shows no hydroxide. Although some carbon is present on the exposed copper,

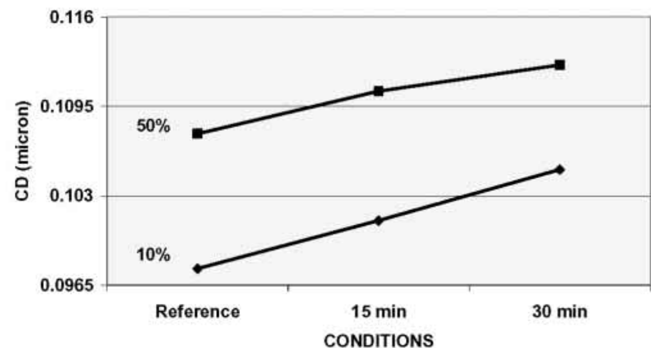
FIGURE 11



CD-SEM measurement of SiLK products following GenSolve 670 removal of etch residue.

FIGURE 12

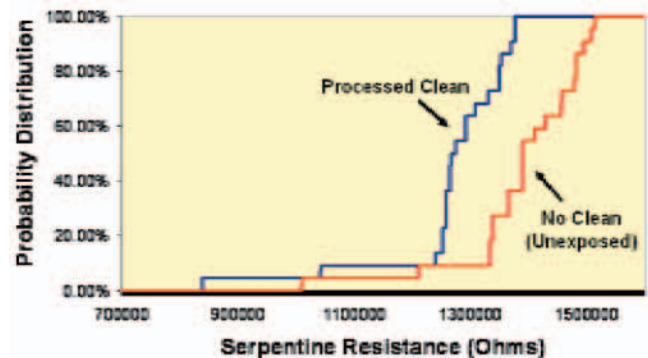
Post Etch of Porous SiLK ILD in GenSolve CD vs Exposure @ 10 & 50% of Line



CD measurement of SiLK porous with exposure to GenSolve 670 taken at 10 percent and 50 percent up the line.

FIGURE 13

Dense SiLk ILD Wafer Electrical Testing Serpentine Resistance, Clean vs. Unexposed



Serpentine resistance measurements for dense SiLK ILD as compared to no exposure (reference).

ESCA/XPS (not shown) indicates it as a nitrogen containing molecule, typical of the inhibitor chemistry used. This surface chemistry appears to impede absorption and reaction of adventitious species. The amount of the identified organic species is on the order of 3 to 5 monolayers, based upon the analysis depth for XPS of 50 to 150 Å, and 40 percent of this signal arises from organic constituents. This very thin protective layer for copper is expected due to the design of the inhibitor to not be a BTA-based system, which has been observed to trigger a continuous coating action.

FEATURE SWELLING AND UNDERCUT

The integrity of the features on the wafer must be verified after chemical exposure. Due to the potential of chemical interactions with the ILD or the substrate, thickness changes may occur over time. Profilometry or ellipsometry may be used to measure such a change. In this study, plated copper substrates were used and measured before and after exposure over a range of time. Table 2 indicates the measured result of copper thickness variation as measured in angstroms per minute.

TABLE 1

Chemistry	Cu Thickness Variation
GenSolve 670	< 0.1 angstrom/min

Copper thickness variation following exposure to GenSolve 670 over a range of time extending to 100 hours

Common areas of focus are the lines and spaces at the smallest location nodes. After chemical exposure, the ILD may undergo absorption and become swelled or bulged. Another issue may be recession (etching) or undercutting. Cross-sectional sample preparation followed by critical dimension (CD) analysis is a means to answer these questions. The SEM photos in Figure 11 show the features from dense and porous SiLK.

Once the CD-SEMs are completed, dimensional analysis occurs and determinations are made regarding swelling and undercutting. Table 2 provides the analysis results from the photos in Figure 11.

TABLE 2

SiLK	Line (microns)	15min (microns)*	30min (microns)*
Dense @ 10%	0.25 (0.18)	0.0078	0.0032
Dense @ 50%	0.25 (0.18)	-0.0024	0.0022
Porous @ 10%	0.175 (0.10)	0.0035	0.0072
Porous @ 50%	0.175 (0.10)	0.0031	0.0050

* Values shown are difference between actual and reference

CD values for the observations in Figure 11. Values reflect the difference between the measurement of the line and reference. The two versions tested are 10 percent and 50 percent (midpoint) up the line from the bottom. Each condition is tested at 5 minute and 30 minute exposures to GenSolve

Table 2 indicates that the node design and actual values vary as described for dense at 0.25 and 0.18 microns, respectively. The same applies for the porous wafers tested at 0.175 and 0.10 microns for design and actual, respectively. The relative CD values noted in table 1 vary between 1 to 6 percent of the total line width. These values are low considering that this etch process is likely not optimized. A graphics representation of the porous part of this data is given in Figure 12.

Successful residue removal for next-generation technology nodes may involve many challenges, yet can be achieved by designing complimentary cleaning tools and chemistries.

ELECTRICAL MEASUREMENT

Following full wafer processing, metallization occurs and the wafers undergo electrical parametric testing. For the SiLK product, subsequent processing and electrical testing was performed by International SEMATECH. As of the date of this publication, no electrical test results were available for the MSQ ILD wafers. Several electrical measurements were performed to include serpentine resistance, sheet resistance, stray capacitance and bridging current. The same measurements were made on a non-exposed (reference) wafer. Figure 13 shows the serpentine resistance measurement for both the processed and unprocessed reference wafers. The processed wafer yields on average a 10 percent decrease in resistance relative to the reference wafer. Reduction in resistance is consistent with sidewall polymer removal. Specifically, as the polymer sidewall residue is removed, the trench linewidth increases slightly, which would result in reduced line resistance. Leakage current and capacitance data (not shown) are consistent with improved electrical performance as a result of cleaning with the GenSolve 670.

PROCESS RECOMMENDATION AND BATH LIFE

In review of the cleaning times studied in both static bench tanks and automated tools, the following process conditions are recommended for etch residue removal from SiLK and MSQ SODs:

GenSolve 670, 60°-70°C, < 30 minutes; DI water rinse + SRD

In most batch spray tools, the stripper will be collected and returned to the heated reservoir where it is brought back up to operating temperature in preparation for the next group of wafers. Reprocessing of the stripper can be carried out for many cycles. The exact number of cycles will depend on the size and number of wafers, tank size and the amount of residue. The bath life, defined as that time or number of cycles determined to provide consistent performance, is high for GenSolve 670

due to its high solubility for both organic and free inorganics leached from the residue. Many simple monitoring tools are available to quantify performance with polymer loading. An added benefit when recycling is the filtration efficiency of GenSolve 670 over semiaqueous materials that may foul the filtering assembly.

BATCH CLEAN TECHNOLOGY FOR NEXT GENERATION

Successful residue removal for next-generation technology nodes involve many challenges, yet can be achieved by designing complimentary cleaning tools and chemistries. Performance, throughput and cost are primary drivers in semiconductor manufacturing, particularly for application-specific IC (ASIC) manufacturers.

Performance is characterized by selective removal of the residue with control of variability across the wafer. This means that the same performance must be witnessed at the edge as observed at the center of the wafer. This can be measured by various techniques to include electrical testing.

Throughput can be optimized by using chemistries with short dispense times. Understanding the limits of the tool and matching a chemistry to that design can result in rapid processing. For example, choosing a lower-viscosity chemistry with surfactants may reduce cycle time and improve rinsing to reduce the overall process.

Using a chemistry in a tool that allows simple water rinsing not only reduces environmental health and safety (EH&S) concerns but also simplifies the process. Further, collection and recycling of material from the process chamber where it may be filtered and prepared for another batch of wafers will improve product usage. Through recycling, the bath life for a particular chemistry may extend to numerous batches, resulting in increased wafer throughput, reduced downtime and lower cost.

CONCLUSIONS

Characterizing residue removal following the etching of SiLK and MSQ based SODs is fundamental to successful integration. Using a range of chemical and physical methods, much information can be obtained to describe product performance and selectivity as well as the ability of the tool to operate within an envelope and provide good uniformity across the wafer. By matching a chemistry to a tool design, the performance and throughput of the process can be optimized for a batch approach. Simplifying the rinse cycle and recycling the chemistry will further reduce process time and improve bath life leading to continued reduction in costs.

ACKNOWLEDGMENTS

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During reactive ion etching (RIE), part of the resist mask is broken down and incorporated into the plasma and distributed over the entire wafer, causing a preferential redeposition into the vias and troughs.

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