MICRO

Using batch spray processing to reduce cycle times and improve performance

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Production and pilot-line data show that an optimized rinse/dry cleaning technique involving batch spray processors can reduce consumption of chemicals and water while lowering cycle times.

A*s the IC industry continues to* fabricate devices at ever-smaller technology nodes, equipment suppliers must optimize existing applications and develop new ones to meet or exceed increasingly stringent manufacturing requirements. Hence, demands have been placed on manufacturers to reduce the consumption of chemicals and DI water and implement processes that rely exclusively on the use of ozone and dilute hydrofluoric acid.[1–3]

New trends in IC manufacturing drive these requirements.[4] One trend is that IC manufacturers have begun to shift from the production of large volumes of a few types of products to the production of small volumes of many types of products. This shift, in turn, has increased the demand for wet cleaning systems that provide shorter cycle times rather than maximum throughput.

Because batch immersion systems were designed to run large batches of wafers to achieve high throughput, they have nearly the same cycle time when processing a single wafer as they do when processing 100 wafers. In contrast, single-wafer systems are designed to process one wafer as fast as is practical to achieve a very short cycle time, generally resulting in relatively low throughput. Batch spray processors offer the advantages of both types of systems, enabling users to process large batches with high throughput or small batches with short cycle times.

The ability to lower chemical and water consumption combined with hardware improvements has resulted in batch spray processor technology from FSI International (Chaska, MN) that reduces cycle times and 65-nm particle levels in front-end-of-line (FEOL) and back-end-of-line (BEOL) applications. Based on work performed at Texas Instruments' DMOS6 300-mm production fab in Dallas, this article discusses process optimization and development efforts involving that technology.

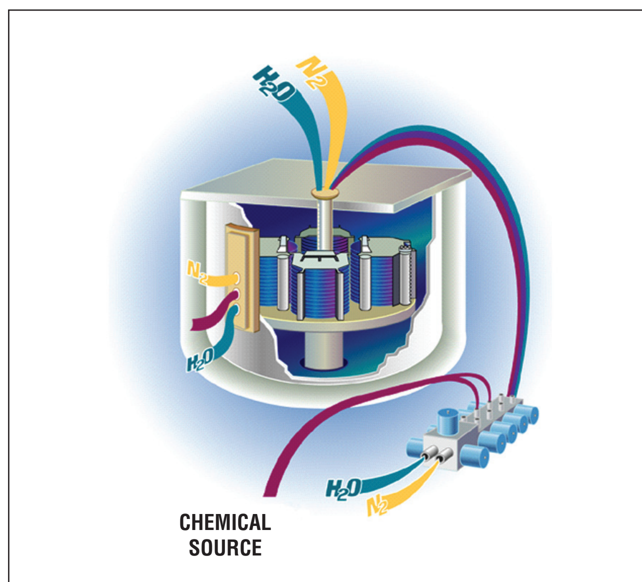

Figure 1: Cross-section diagram of a Zeta spray processor showing the tool's mixing manifold, which is used for delivering chemicals, DI water, or nitrogen to the process chamber.

Spray Processor Technology

Spray processors are dry-in/dry-out wet cleaning systems that can be used at virtually all wet cleaning steps for both FEOL and BEOL applications. Batch spray processors are typically configured with up to eight chemical inputs, a DI-water input, and up to two recirculation systems. Chemicals can be dispensed individually, or they can be mixed with one another and/or with DI water. Once mixed, the chemicals are dispensed onto the wafers in a process chamber, as illustrated in Figure 1. Because of their flexibility, spray processors can be used to generate a wide range of chemical mixtures that can be dispensed at ambient temperature or heated with an onboard infrared chemical heater. The recirculation system can dispense many FEOL chemicals and BEOL class III solvents with flashpoints above 60°C.

Spray processors have several advantages. They typically have a smaller footprint than immersion tools because processing is performed in a single chamber. All chemicals dispensed onto the wafer surface are either fresh or freshly filtered. Since the wafer is rotated during the cleaning process, centrifugal force enhances particle removal efficiency and overall rinsing efficiency. Spray processors' enhanced rinsing efficiency results in less overall DI-water consumption than that achieved with comparable immersion processes.

Process Improvements

When manufacturing processes were transferred to 300-mm production lines four years ago, recipes were copied as closely as possible from 200-mm equipment. After initial qualification, development work began to take advantage of the improved design and process capabilities of the 300-mm systems to reduce process times and DI-water use.

Rinses between chemical dispense steps in a multiple chemical process sequence are a large contributor to DI-water consumption and cycle times. For example, rinsing sulfuric acid, a relatively viscous chemical that is used in high concentrations to strip photoresist, requires large quantities of water and is time-consuming. Studies have focused on special techniques to reduce the volume of rinsewater needed following sulfuric acid steps.[5] Most other chemicals, including HF, NH_4OH and HCl, are much easier to rinse because they are used in dilute mixtures with DI water. Rinsing steps following the use of more-dilute chemical mixtures are therefore good candidates for optimization.

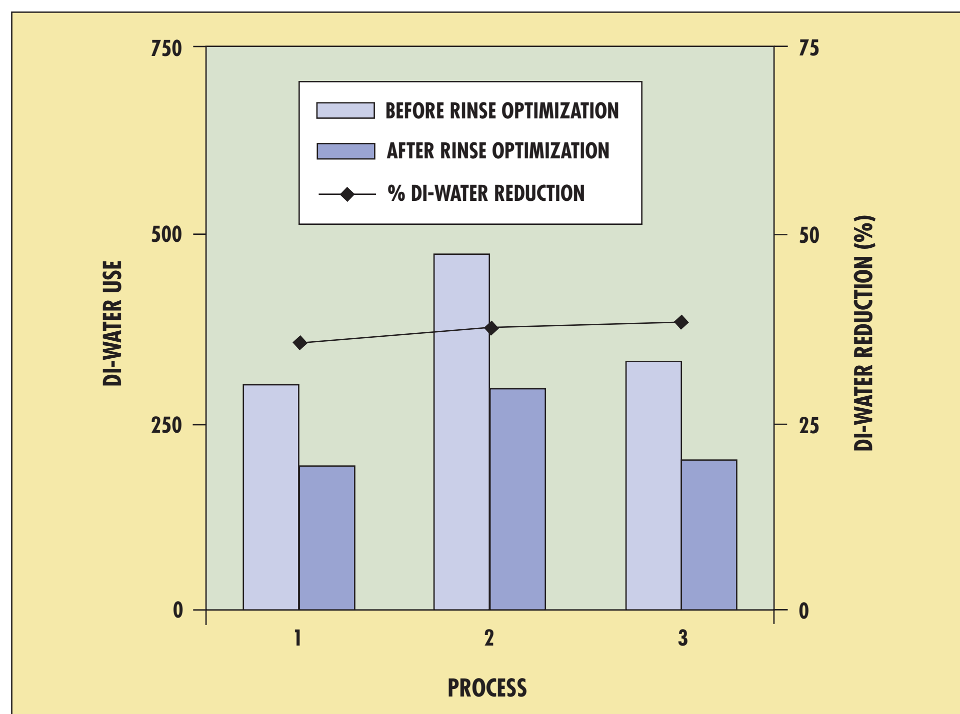

Figure 2: Rinsewater consumption in a 300-mm production facility before and after a first round of process optimization.

When processes were transferred from 200- to 300-mm equipment, chemical dispense steps were copied exactly from old recipes. At the same time, drying steps were scaled up because the larger wafer and chamber sizes increased overall drying times. Therefore, manufacturers and toolmakers

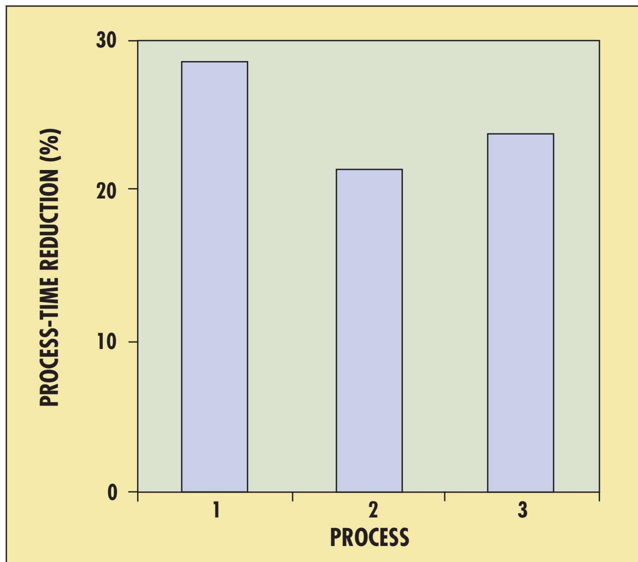

Figure 3: Process-time reductions achieved after the implementation of an optimized rinsing process in a 300-mm production fab.

Process Step	Original Process Time (min)	Reduced Process Time (min)
Preheat	3	3
Piranha	12	12
Postpiranha rinse	12	5
SC-1	8	12
Post-SC-1 rinse	6	—
Final rinse	3	3
Dry	10	7
Total time	54	42

Table I. Representative FEOL photoresist removal process improved through reduced rinsing and drying. By reducing the rinsing time, overall process cycle time was reduced by 22%.

sought to reduce rinse times between chemical dispense steps in order to improve the final rinse-and-dry sequence without changing the chemical steps. The results of such efforts are presented in Figure 2, which shows that the use of batch spray processes, with optimized rinse-and-dry sequencing, lowered water use by 35 to 40%. Figure 3 indicates that in the same facility, optimized rinses reduced process times by 20 to 30%.

Optimized rinse recipes were qualified and implemented in a 300-mm production line. The list of standard photoresist-removal steps in Table I demonstrates that the optimized process sequence resulted in a 22% reduction in cycle time and a significant reduction in water consumption. Particle level, inline defect density, multiprobe yield, and electrical performance data indicate that the wafers from the first optimization round were as good as those from the older process generation.

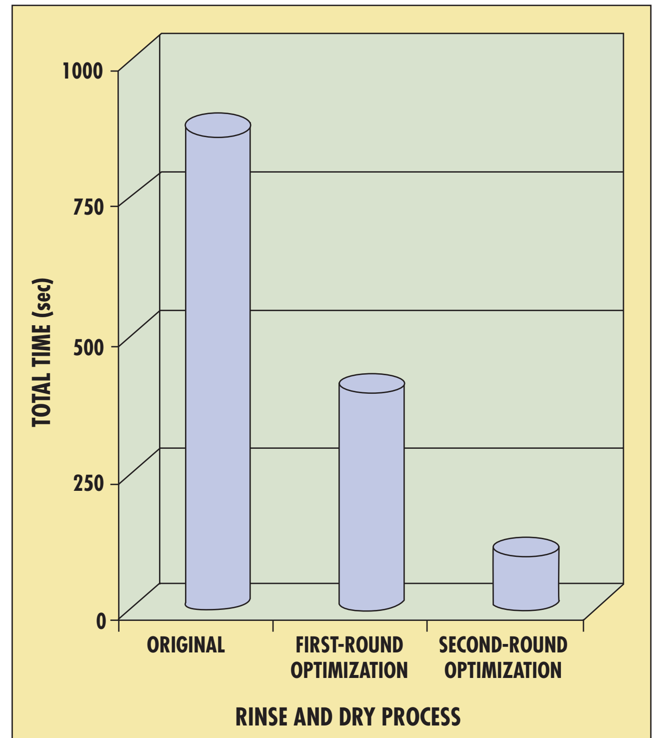

Figure 4: Drying-time reductions achieved after the first round of process optimization and after the implementation of the rinse/dry process combined with a hot chamber rinse.

Optimizing Cycle Time and Process Performance

In the second optimization round, the goal was to improve productivity and 65-nm defect performance. This optimization, known as FlashClean Advantage, resulted in a process sequence that includes a new final rinse-and-dry sequence and a minor hardware modification of the spray processor.

Final drying in a batch spray processor is traditionally accomplished by using high flow rates of nitrogen at the end of the process sequence. This nitrogen purge, performed while the wafer spins rapidly, forces water into a very thin sheet, allowing it to evaporate over the course of 5 to 10 minutes. While this technique has been standard in batch spray processing for many years, new methodologies have resulted in improved defectivity levels for particles <120 nm.

The transition of the wafer surface from wet to dry was recognized as the key point to improve process performance, since there was a strong correlation between particle performance and wafer temperature at the end of the process. Traditionally, the lowest defectivity level is achieved when wafer temperatures are 5° to 10°C above the ambient temperature.

To understand how the final evaporation of water from the wafer surface affects defect levels, three variables were investigated: chamber temperature, nitrogen flow rate, and platen rotation speed. A variety of experiments were conducted using 90-nm particle adders as the response variable, resulting in an optimized rinse-and-dry sequence that

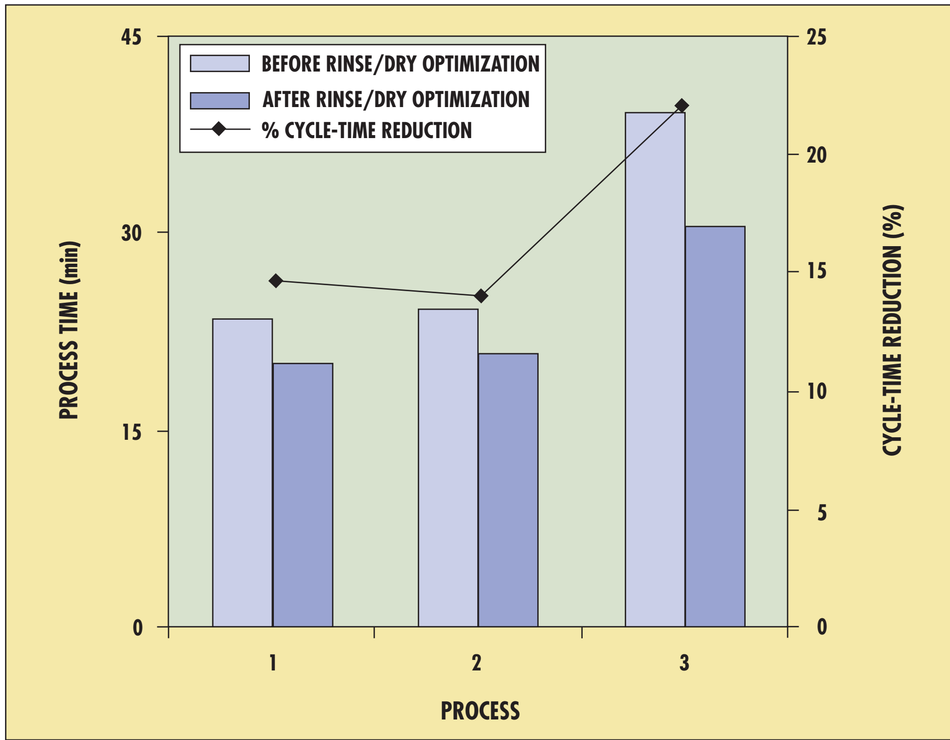

Figure 5: Process-time reductions achieved after the implementation of the rinse/dry process combined with a hot chamber rinse and hardware changes.

remained the baseline for nearly three years. As defect monitoring shifted to 65 nm, however, it was recognized that further improvements could be obtained.

Once again, investigators focused on the transition from a wet to a dry wafer. In particular, they determined that most 65-nm defects were added during the 10-second interval in which the DI-water rinse lines are purged onto the wet wafer. Hence, they decided that it was necessary to aspirate instead of purge the final rinse line, resulting in near-particle-neutral defect levels down to 65 nm.

While the transition from final rinse to dry steps was under investigation, investigators were developing the capability to dispense hot rinse water onto the walls of the process chamber. Rinsing the process chamber with hot water enables the tool to achieve significantly lower final drying times. The chamber-rinsing process was accomplished by dispensing water from the rotating platen, which required a rotary water feedthrough and, therefore, a new hardware design.

Figure 4, which shows drying times for 50 300-mm wafers, illustrates that the process optimizations culminating in the new rinse/dry sequence combined with a hot chamber rinse have greatly lowered the final time required to dry wafers in a batch spray processor. Figure 5 shows how the use of this system in three different 300-mm processes has resulted in a 14 to 22% reduction in overall process time.

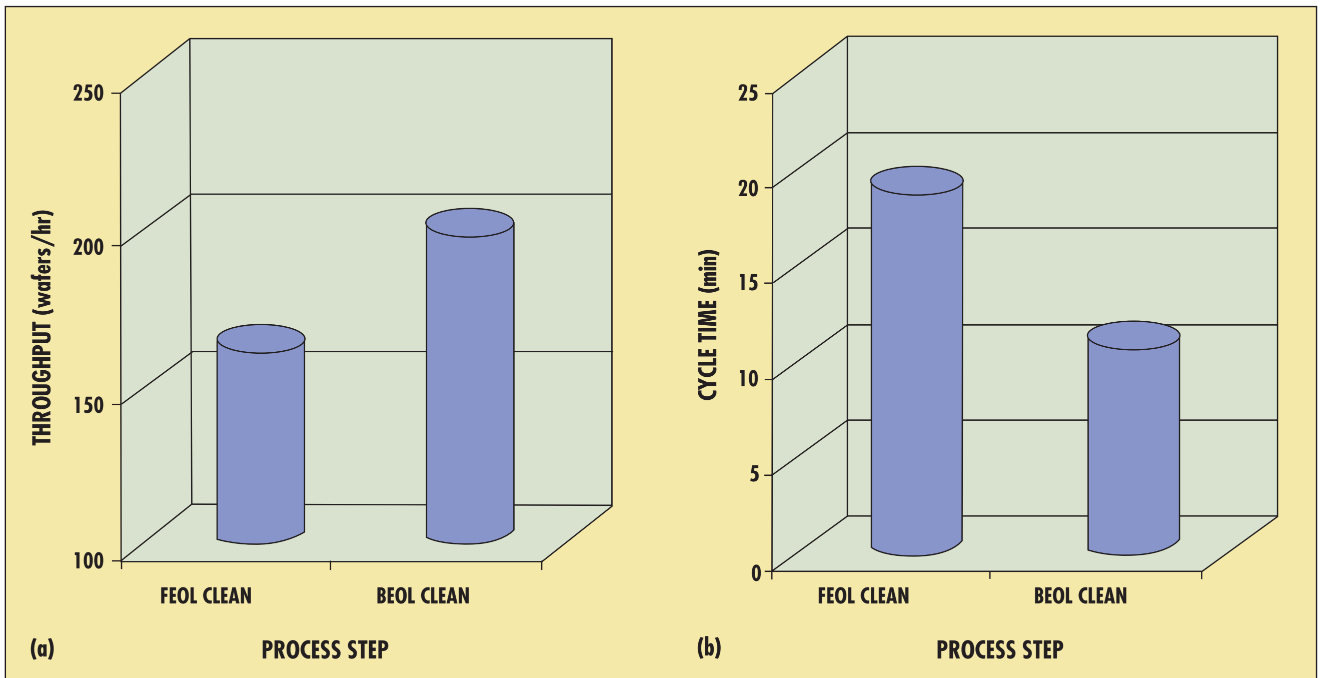

Figure 6: Data from FEOL and BEOL postash residue-removal processes showing (a) throughput for 50-wafer batches, and (b) cycle time for 5-wafer batches.

Sum of All Defects >65 nm			
Preclean	Postclean	Δ	True Adders
284	81	–203	14
554	62	–492	12
569	64	–505	9
706	61	–645	6
737	52	–685	11
787	73	–714	12
944	93	–851	20
1001	70	–931	11
873	62	–811	10
950	52	–898	7

Table II: After 10 new 300-mm wafers were cleaned, the total count of all defects >65 nm fell to between 50 and 100.

Coupling Large-Batch Throughputs and Small-Batch Cycle Times

Figure 6 summarizes throughput and cycle times for FEOL and BEOL postash cleaning processes using the rinse/dry process optimization. FEOL piranha/SC-1 cleans typically provide a throughput of 160 wafers/hr for 50-wafer batches and a 20-minute cycle time for 5-wafer batches.

A 20-minute cycle time for piranha/SC-1 cleans is not revolutionary; in fact, it is too slow to be transferred to single-wafer platforms. While important work has been performed to find alternatives to that cleaning method, no proposal has been widely accepted.[6] Additionally, the concern that surface modifications can result from the adsorption of surfactants during FEOL cleaning applications may be a strong barrier to the acceptance of new chemistries.[7] And as gate oxide thicknesses continue to shrink, the impact of potential contaminants will become even greater.

A study demonstrating that single-wafer chemical formulations work well in batch spray processors has also shown that spray processor technology can remove BEOL residues completely in 1 minute.[8] The BEOL postash process highlighted in Figure 6 was completed in 1 minute and consumed less than 5 ml of chemicals per wafer. That study dispels two common myths: first, that batch processors require long chemical exposure times; and second, that single-wafer and batch processors require different chemicals.

Statistical Parameter	Standard Clean	Optimized Clean
Upper control limit	213.6	24.4
Mean	44.5	1.2
Lower control limit	–124.5	–22.1

Table III: Statistical breakdown for data shown in Figure 7.

Particle Performance

The optimized rinse/dry process substantially improves particle performance down to 65 nm. At the 65-nm particle level, incoming wafer quality is a concern. Typically, new, as-received wafers have varying levels of surface particles and contaminants. Some wafers become contaminated in the shipping container, while others remain clean. In any event, all new wafers must be cleaned or conditioned before use, and one of the best means of accomplishing that is a piranha/SC-1 postash clean. Table II presents the results of cleaning 10 brand-new 300-mm bare silicon wafers using a piranha/SC-1 clean. True adders are particles deposited by the tool or moved and redeposited by the cleaning process.

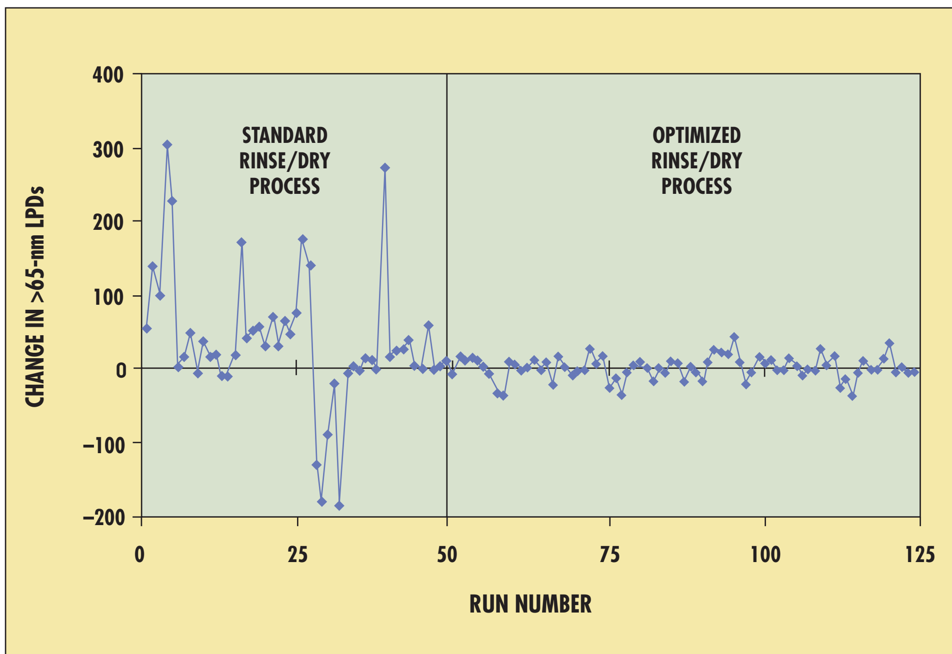

Figure 7: Data for 300-mm wafers with a 2-mm edge exclusion showing light-point defects >65 nm from an FEOL postash cleaning process before and after rinse/dry optimization. Each data point represents an average of three wafers.

Figure 7 compares FEOL postash cleaning data from an FSI 300-mm Zeta spray processor that ran both a standard rinse/dry sequence and the optimized rinse/dry process combined with a hot chamber rinse. In both cases, the same cleaning recipe was used, ex-

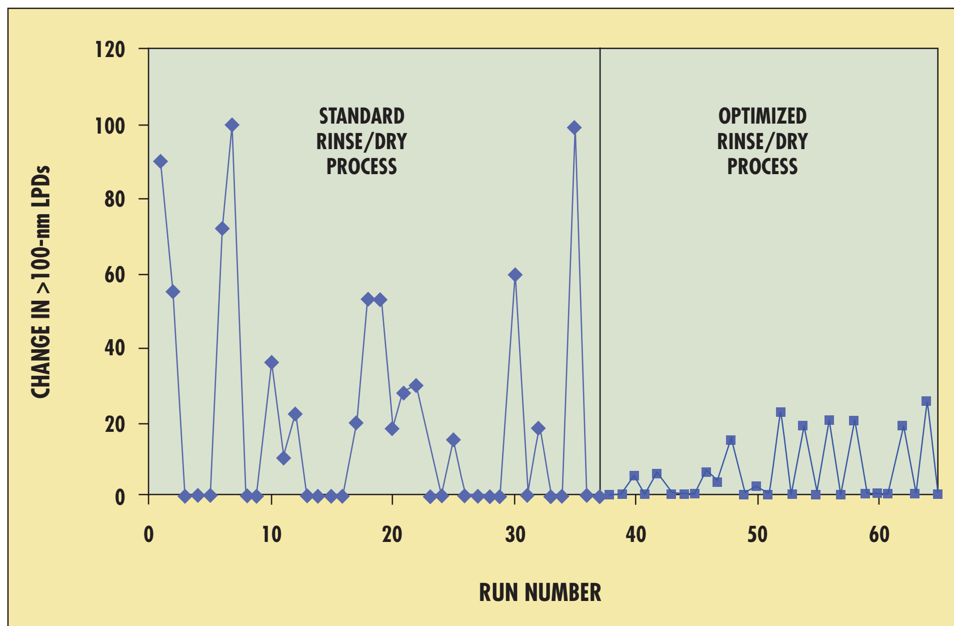

Figure 8: Pilot-line data for 300-mm wafers (3-mm edge exclusion) showing light-point defects >100 nm from an FEOL postash clean before and after rinse/dry optimization.

cept for the final rinse/dry sequence. Table III shows the upper control limit, mean, and lower control limit for the data in Figure 7. The data reveal that the optimized process resulted in better performance for light-point defects >65 nm than the standard process.

The data in Figure 8, for a system installed in a 65-nm pilot line, are similar to those presented in Figure 7. Based on daily qualification performance, they show that after the optimized rinse/dry process was implemented, light-point defects >100 nm declined substantially.

Conclusion

Changing market needs led a toolmaker to improve process performance, resulting in cleaning methods that conserve materials and reduce cycle times. These improvements were qualified on 300-mm production lines. Cycle-time reductions in the range of 10 to 25% have been achieved for both FEOL and BEOL processes. Cycle times for small wafer batches in a BEOL postash residue-removal process can be as short as 11 minutes. The upper control limit for tests measuring the number of particle defects >65nm has been shown to be under 25 for a range of applications.

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