

HF Based Cleaning Processes for Current Applications and New Materials in an Advanced Immersion Cleaning System

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Biography

Nam-Pyo Lee is a Member of the Technical staff at FSI International. He received his M.S. degree in chemical engineering from Kyunghee University in Korea. Prior to joining FSI, he worked as a cleaning development engineer for Samsung. Since joining FSI International in 1996 he has been working wafer cleaning application development especially for HF vapor cleaning, spray chemical cleaning, and STG (Surface Tension Gradient) drying.

Steve Nelson received a B.S in Physics and a B.S. in Mathematics from the University of Minnesota in 1992. He is a senior applications development engineer for FSI International Inc. in the Surface Conditioning Division. His responsibilities include development of Ozone cleaning process development of immersion cleaning processes. He is a member of the Electrochemical Society where he has published numerous articles and had numerous presentations.

Abstract:

Diluted HF “cleans” (DHF) is the most widely used cleaning method in semiconductor processing. It is intended to remove one nanometer of native oxide or a few nanometers of bulk SiO₂, and thus expose and remove any metallic contamination that are present in these oxides. DHF surface preparation is used to create a hydrogen-terminated silicon surface that is low in oxygen in preparation for gate growth or contact metallization.

Controlling the HF process is one of the most difficult tasks, especially for 5mm-spaced 300mm silicon wafers. In order to avoid particle deposition, control precise oxide etching, and process various materials such as low-k and high-k it is important to utilize an advanced hardware and software technology.

A fully automated and flexible immersion processor has now been designed, built and characterized for processing 300mm silicon wafers in DHF-based applications.

Characterization of the equipment has included particle performance of the DHF last process, thin thermal oxide etching uniformity, and particle migration control from an oxide wafer separated by 5mm from a silicon wafer during HF process.

Processes have been developed for new applications including super-hydrophobic materials such as carbon-doped low-k and thin chemical oxide thickness control for high-k dielectric deposition.

Experimental Setup:

The FSI Magellan[®] 300 STG[®] Immersion Clean System was used in these studies. The system allows chemical processing in the rinse/dry tank using SymFlow[™] technology for high-uniformity HF-last, controlled thin chemical oxide DIO₃, and metal contamination free HF-dHCl processing. The system architecture performs dilute HF etching in the same tank as the final rinse and dry, while maintaining a low-oxygen environment, keeping the wafers completely immersed until the IPA vapor surface tension gradient drying is complete.

It is very important to develop an efficient rinse process so the rinse time will be short, maximizing the number of wafers that can be processed and minimizing the amount of water used. Figure 1 shows data for different rinse times using newly developed sparger-bars for chemical collected from within 8.9- μ m from the wafer surface (1). The rinse efficiency within 8.9- μ m of the wafer surface is found to be 88.8%, which is a high rinse efficiency. This means that the boundary layer at the wafer surface is very thin during rinsing.

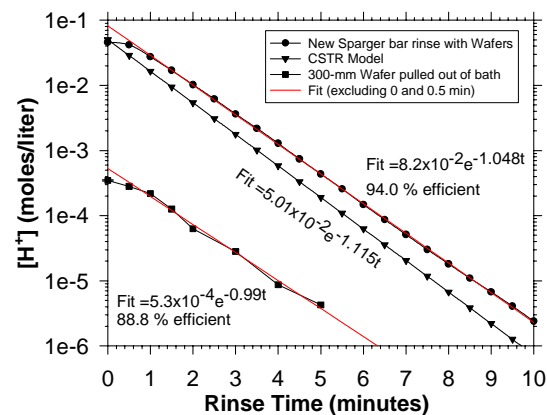


Figure 1: Overflow and on-wafer pH data for new sparger-bar rinsing at 39.5-lpm.

Figure 2 shows the oxide etch uniformity for different rinse times using the new sparger-bar setup and a rinse flow of 40-lpm after soaking in 200:1 HF.

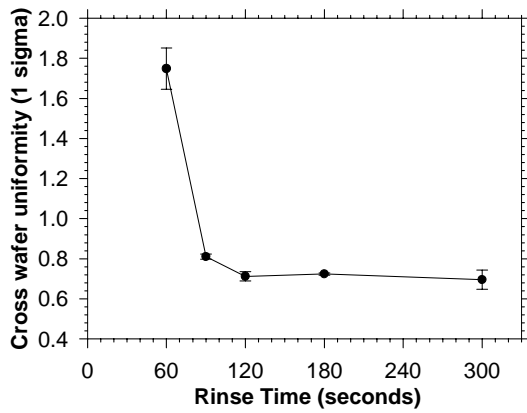


Figure 2: Affect of optimized rinse time on oxide etch uniformity

Figure 3 shows the affect of rinse time on the number of particles added to clean silicon wafers after a 120-second soak etch in 200:1 HF.

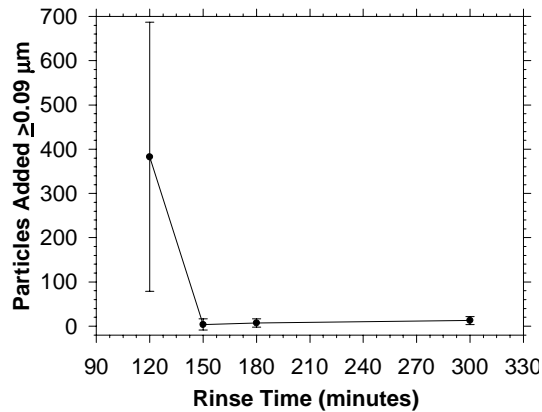


Figure 3: Affect of optimized rinse time on particles added

Based on data collected after a 200:1 HF etch, the rinse time was set at 180 seconds. However, the post HF rinse time may need to be adjusted based on the electrical tests of product wafers.

In an STG[®] dry, the rinse water is slowly drained at 2 mm/sec depending on device conditions from the closed rinse tank and dried using a low concentration of IPA vapor in nitrogen.

To check the oxide etch uniformity, oxide wafers were precleaned with an SC1 process and placed in the front, center, and back slots with filler wafers in all the other slots in the cassette. A Rudolph Caliber 300 ellipsometer was used to measure the oxide thickness. 49 points were scanned with 3mm edge exclusion on the wafers.

Particles were measured on silicon wafers using a Tencor SP1 TBI with the oblique laser to illuminate the particles. Particle density was generally measured for sizes greater than 90nm. Some measurements were made for sizes greater than 60nm. For low-k materials, particles were

measured for sizes greater than 120nm.

Results:

HF last particle performance is shown in Figure 4 and 5. This data was collected from 5 consecutive runs for particle addition at >90nm. Particle addition at >60nm was also collected from additional 5 consecutive runs. The data clearly show superior performance of the STG[®] dryer on hydrophobic wafers at both 90 and 60nm particle size.

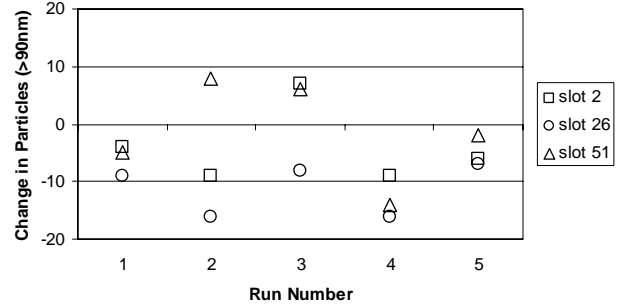


Figure 4: Results for SC1-HF-R/D with 300mm wafers. Average starting counts were 31 at >90nm

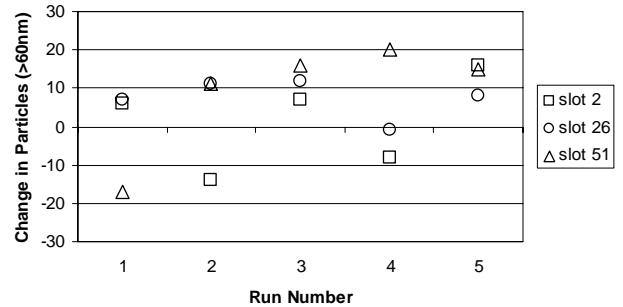


Figure 5: Results for SC1-HF-R/D with 300mm wafers. Average starting counts were 90 at >60nm

Thin Oxide Etching Performance

In immersion systems, dilute HF (DHF) etches have traditionally been performed in a conventional dual-tank approach by immersing a batch of wafers in a pre-mixed DHF etch tank supplied from a pre-mixing tank and then rinsing the wafers by cascading DI water.

A new thin oxide etching process by introducing DI water through arrays of small holes in sparger bars located at the bottom of the tank has been developed and shows that a single-tank process can achieve and provide better uniformity. The process sequence is as follows:

1. Immerse the wafers in DI water
2. Flow DI water to establish a stable fluid profile
3. Inject HF into the DI flow stream
4. Continue the HF flow up to desired etch target
5. Stop HF flow and allow the continuing DI flow

This symmetrical rinse-etch-rinse process produces a more uniform etch profile. In addition, the process reduces tool complexity and footprint through elimination of the metering pump, pre-mixing tank, and delivery system.

A result of thin oxide etching performance is shown in Figure 6. At an etch amount of 3nm, the average within wafer uniformity is 0.8%, 1sigma with an average within wafer range of 1.3Å.

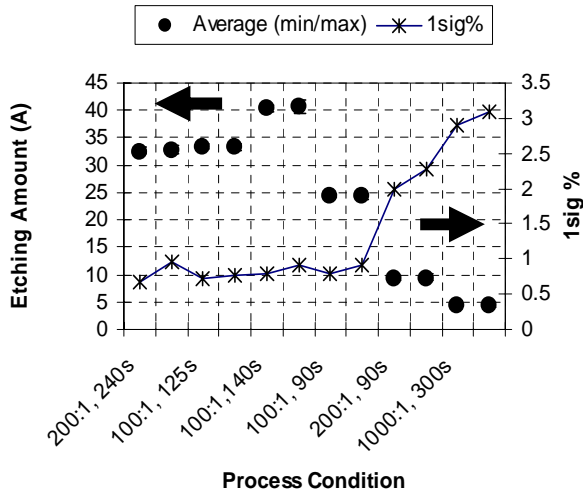


Figure 6: Thin Oxide Etching Performance as a function of Blend ratio (DI:49% HF) and Process Time

Cross Contamination Control Performance

It is well known that when oxide and bare silicon wafers are placed together in same batch, oxide particles migrate onto the bare silicon surface in an HF etching process due to the electrostatic interaction between particles and wafers. A typical particle migration pattern is shown in Figure 7.

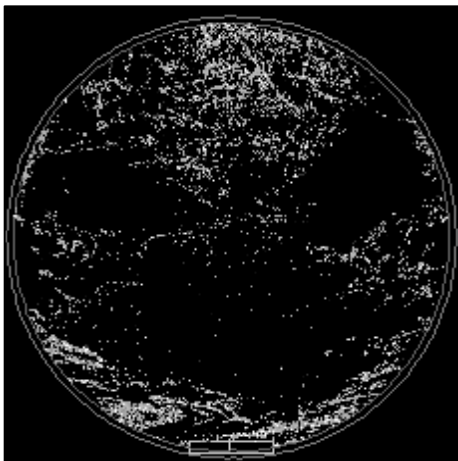


Figure 7: A typical particle migration pattern after 30A oxide conventional etching process (pre count: 84 at >90nm).

Since patterned wafers have hydrophobic and hydrophilic areas it is important to optimize the drying process when having both surface types especially for wafers at 5mm-spaced pitch.

After various investigations, it was found that the oxide particle migration issue can be resolved by controlling key process parameters in the final rinse/dry step. Particle migration test results from two different demonstrations are shown in Figure 8.

after HF process are shown in Figure 9. A hydrophobic bare silicon wafer was placed one slot away from an oxide wafer. Test was done to show that there was no contamination from the etching of the oxide wafer.

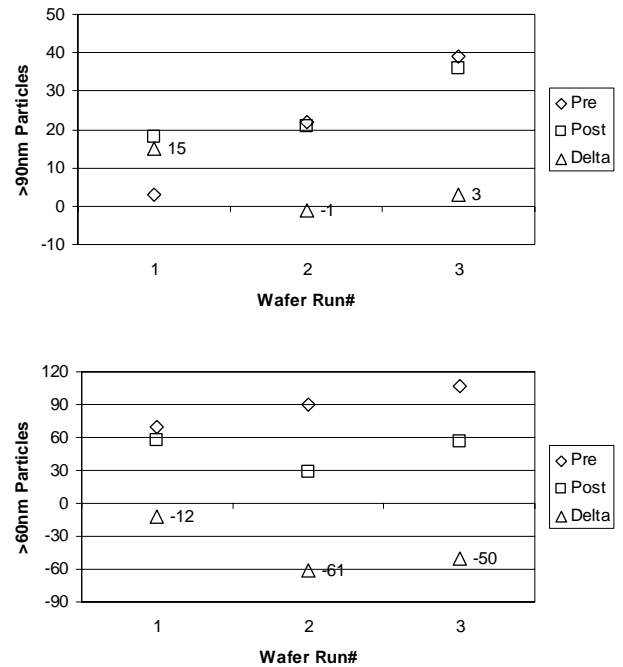


Figure 8: Particle migration demonstration results from customer A (top, average starting count: 21) and customer B (bottom, average starting count: 89)

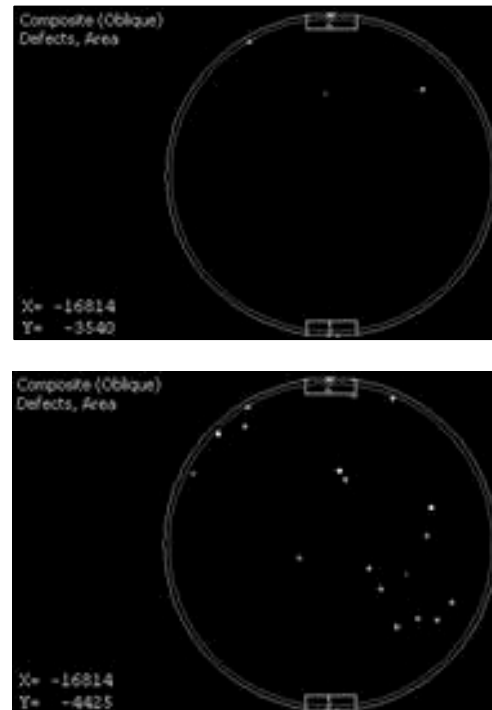


Figure 9: Particle distribution maps at >90nm before (count: 3) and after (count: 18) HF process

Super Hydrophobic Surface Drying

As minimum device features shrink below 180nm copper and low-k dielectrics are being combined to overcome interconnect resistance and capacitance delay. Since low-k is moving toward more porous and carbon base material, which are known to be super-hydrophobic, advanced drying technology becomes important. From a cleaning point of view, the surface cleaning of low-k material is still under development. For the investigation of drying performance on low-k films, Coral was studied as the test materials. Figure 10 shows a typical drying pattern on low-k materials after rinse/dry.

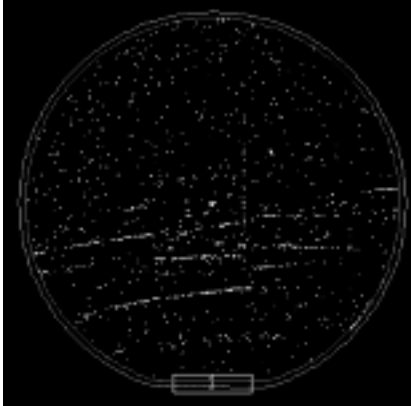


Figure 10: A typical drying patterns on low-k material after rinse/dry process

Coral films were given a rinse only and an dHF followed by rinse and then dried on the STG® process tank with optimized process conditions. Figure 11 shows particle performance from Coral. After processing no drying pattern was observed from the Coral films.

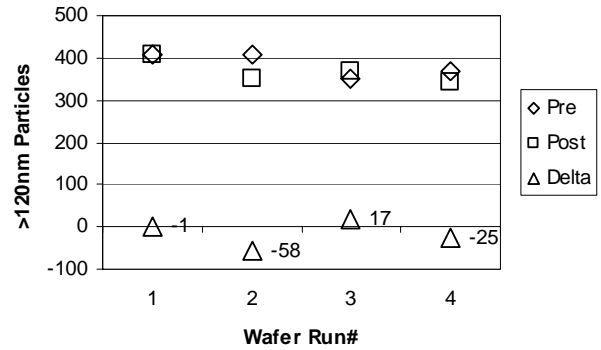
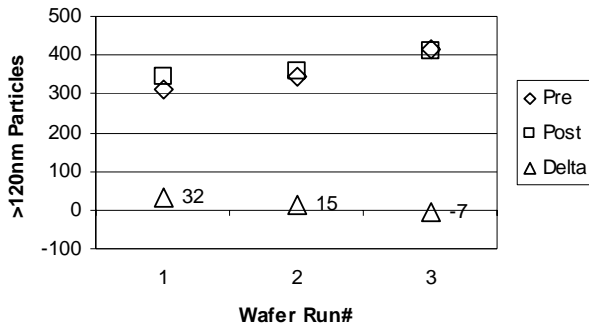


Figure 11: Particle performance on Coral from rinse/dry only (top) and HF followed by rinse/dry process in the rinse/dry tank (bottom)

Thin Chemical Oxide Control for High-k dielectric Deposition

It has been found that it is most desirable to deposit the new high-k gate dielectric films on an oxygen passivated surface rather than on a bare silicon surface. A thin surface oxide provides better electrical properties at the silicon-high-k interface. However, if the oxide layer is too thick or non-uniform, it will eliminate the advantages of the high-k dielectric film. Being able to control the chemical oxide thickness prior to high-k deposition allows for optimization of the electrical properties.

Figure 12 shows how the chemical oxide thickness is affected by the ozonated water dispense time at a constant ozone concentration of 40 ppm at room temperature. The chemical thickness increases until it is 10Å thick and then stops growing. Once the chemical oxide reaches its maximum thickness, the oxide becomes more uniform across the wafer and cassette, as can be seen by the decrease in the %1 sigma. The figure also shows very unstable thickness until it reaches the maximum thickness.

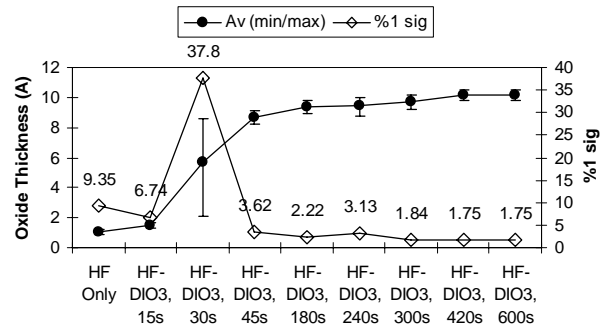


Figure 12: Non-uniformity vs. oxide regrowth thickness with conventional method

To control the oxide regrowth thickness in a range of 4 ~ 8 Å, a new ozone concept is demonstrated. Figure 13 shows the results of oxide regrowth thickness controlled by the

new method. The average oxide regrowth thickness was 5.6\AA with an average within wafer range of 0.37\AA . Within wafer uniformity was 1.4%, 1sigma.

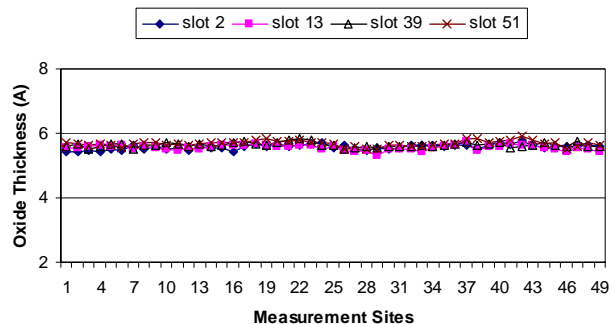


Figure 13: Oxide regrowth thickness controlled by a new method – 5.6\AA (WIW range: 0.37\AA , 1.43% in 1sig)

Conclusion

A fully automated and flexible immersion processor has now been designed, built and characterized for processing 300mm silicon wafers in DHF based applications.

Characterization of the equipment has included particle performance of the DHF last process, thin thermal oxide etching uniformity, and particle migration control from an oxide wafer separated by 5mm from a silicon wafer during HF process.

Processes have been developed for new applications including super hydrophobic materials such as carbon-doped low-k and thin chemical oxide thickness control for high-k dielectric deposition.

Acknowledgments

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References

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