

Single-tank processing demonstrates immersion batch cleaning for 65nm ICs

OVERVIEW

An advanced batch immersion system for wafer cleaning applications has been tested in 65nm pilot-line production. The fully automated tool incorporates the latest wet-cleaning technology for short cycle-time, single-tank processing while maintaining the high-throughput advantage of 50-wafer batch systems and incorporating production-proven surface-tension gradient wafer-drying techniques. Pilot line tests demonstrated capabilities for low-particle HF-last cleaning, uniform thin-oxide etching, and uniform polysilicon etching. A new process for producing a very thin and uniform oxide layer for high-*k* dielectric precleaning also has been demonstrated.

Characterization of the equipment has included low-particle DHF-last processing, uniform thin etching of thermal oxide, and uniform etching of polysilicon using HF and SC1-HF sequences in a flexible hardware and software configuration. Processes have been developed for new applications, including chemical oxide etch-back grown by DIO3 for high-*k* application and polysilicon etching.

System description

Wafer-cleaning and surface-preparation technology continues to evolve in concert with new materials and processes. Batch technology also continues to be used extensively in semiconductor manufacturing because it has been more cost-effective than single-wafer technologies for many cleaning and surface preparation applications. However, recent advances in single-wafer system designs and process optimization have improved throughput and lowered cost. At the same time, advances in batch technology also have been implemented to improve process performance and reduce footprint [1]. Batch immersion processing, the most common method for wafer cleaning, has been redesigned and optimized for sub-100nm technology nodes as stricter process tolerances are required.

A new batch, single-tank process has achieved excellent uniformity in critical dilute HF (DHF) etching, and has provided better uniformity than the traditional dual-tank process [2] as well as metallic-free dilute HCl cleaning. This symmetrical, continuous flow, single-tank process eliminates the need for a dedicated HF bath, leading to smaller tool footprint. In cases where ammonium hydroxide-hydrogen peroxide (SC1) or ozonated DI water (DIO3) steps precede the DHF step, an additional dedicated rinse-tank bath can also be eliminated. When implemented as part of a prediffusion cleaning sequence, the single-tank approach can reduce the number of cleaning and rinsing tanks from six down to two, cutting the overall tool footprint in half [3]. In addition, in-line chemical blending technology has provided a wide range of mixing capability covering today's conventional processes to future processes, such as high-*k* and silicon-germanium (SiGe) cleaning. The immersion batch-cleaning system, configured as a 200mm bridge tool designed for 300mm wafer processing lines, was demonstrated at a leading IC manufacturer based in Korea, which performed rigorous process-capability testing.

This work was performed on the FSI Magellan immersion clean system, which provides dilute chemical processing in the rinse/dry tank using a patent-pending technology called SymFlow. The system architecture performs DHF etching in the same tank as the final rinse and dry, while maintaining a low-oxygen environment. This setup keeps the wafers completely immersed until the isopropyl alcohol (IPA) vapor surface-tension gradient drying is complete.

SC1 cleaning is carried out in an advanced tank design. The SC1 solution has been used for many years to remove particle contamination with a combination of surface etching and favorable pH. With the semiconductor industry moving to smaller gate linewidths, controlling the amount and uniformity of Si and SiO₂ etching during SC1 processing has become extremely critical. To get the best uniformity, it is important to develop efficient rinse methods so the rinse time will be short, maximizing throughput and water consumption. Historically, dump rinsing has been performed to rinse hydrophilic wafers in a shorter period of time and to lower impurity levels, compared to overflow rinsing. The advanced SC1 quartz tank design combines efficient in-tank mixing with dump/spray rinsing to achieve high throughput and low overall water consumption [4]. This tank also provides for single-pass, single-run, or recirculated chemical processing.

In this study, thermal oxide and polysilicon-coated test wafers were first precleaned using an SC1 process. These test wafers were placed in full, 50-wafer batches along with filler wafers. Oxide and polysilicon thickness measurements were made with an automated ellipsometer using both 49-point and 25-point measurement patterns. Surface-defect density measurements were made for defect sizes >100nm on unpatterned silicon wafers using a laser light-scattering system.

Particle performance

In the FSI surface-tension gradient (STG) rinse/dry process, the

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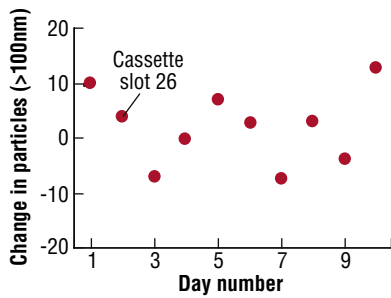


Figure 1. Wafer-cleaning results for SC1 in a quartz tank followed by DHF (200:1, 110 sec) and rinse/dry in the surface-tension gradient (STG) rinser/dryer for 10 consecutive days. The average change in particles was two, with average starting counts of 14 at >100nm.

Three processes were tested for particle performance: a single-tank process of in situ dilute HF followed by STG rinse/dry; a two-tank process of SC1 in a quartz tank followed by STG rinse/dry; and another two-tank process of SC1 in a quartz tank followed by in situ dilute HF and STG rinse/dry in the rinse/dry tank. The particle results for the SC1-HF process are shown in Fig. 1. Similar results were obtained for the other two processes as well. These data clearly show superior performance of the surface-tension gradient STG dryer on both hydrophobic and hydrophilic surfaces.

While particle performance in wafer cleaning is important, water spot performance is the most critical parameter for evaluating drying techniques. The in situ HF-last process also was evaluated using customer-standard water-spot test pattern wafers. The trench-patterned wafers were first cleaned in 200:1 HF for two minutes, followed by the STG rinse/dry, and then inspected using electrical microscopy. It is important to note that electrical microscopy is an effective tool to detect any water spot by comparing site-to-site differences before and after processing. The microscope is able to detect water spot sizes >0.1µm. In this case, nine wafers were fully inspected. No water spot defects were found on any of the wafers.

Etching performance for thin layers

As device geometries approach the 60nm dimension, stricter etch control is a requirement. Etch capability is an important parameter in the comparison of single-wafer and batch systems. In immersion systems, DHF etches have traditionally been performed in a conventional dual-tank approach by immersing a batch of wafers in a premixed DHF etch tank supplied from a premixing tank, and then rinsing the wafers by cascading DI water.

A new single-tank, thin-oxide etch process has been developed [2]. Most etch nonuniformity occurs during the transition of the wafers into, and later out of, the DHF tank, when local time-dependent variations in etchant concentration cause local variations in etch rate. Incoming nonuniformities result from the finite insertion time of the wafers into the bath; the bottoms of the wafers are exposed to DHF approximately 1 sec before the tops of the wafers. This extra 1 sec exposure to DHF results in a systematic 1% cross-wafer variation for a 100 sec etch. These problems have been solved in the new single-tank process by fully immersing the wafers in DI water before injecting DHF solution through arrays of small holes in sparger bars located at the bottom of the tank. At the end of the DHF step, DI water is introduced once again through the same sparger bars. The well mixed, symmetrical flow generated by the

rinse water is slowly drained by a controllable drain valve after post-HF rinsing and is replaced by a low concentration of IPA vapor in heated nitrogen. To evaluate the drying performance, a number of criteria were tested in the IC manufacturing pilot line.

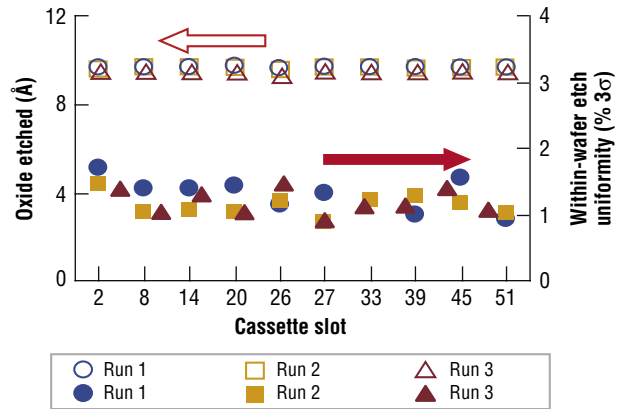


Figure 2. Thin-oxide etching results for DHF (500:1, 255 sec) in the STG rinser/dryer. The sample size was three runs with 10 oxide-etch monitor wafers in each run. An average of 9.6Å of oxide was removed. The average within-wafer uniformity was 1.22%, 3σ; wafer-to-wafer uniformity was 0.67%, 3σ; and run-to-run repeatability was 1.38%, 3σ.

well controlled hardware and software configurations produces a more uniform etch profile. In addition, this approach reduces tool complexity and footprint by eliminating the metering pump, pre-mixing tank, and delivery system needed for a separate, recirculated DHF tank. Results of thin silicon dioxide etch performance are shown in Fig. 2.

With a traditional recirculated DHF tank, the DHF can be diluted locally by the incoming carryover layer of water from the previous rinse. It was found that dry wafers inserted into the DHF bath etch more uniformly than wafers that were wet from a preceding SC1 step. By fully immersing the wafers in nonreacting DI water before introducing DHF, the carryover dilution effect is completely eliminated. Fig. 3 shows results of the process for DHF etching after an SC1 step.

Since the continuous scaling of ICs also demands a minimum of polysilicon loss with good uniformity during SC1 processing, it is highly desirable to have advanced and flexible configurations for the SC1 quartz tank. The system can be configured with up to eight chemical inputs. Chemicals can be dispensed individually, or they can be mixed with one another and/or with DI water.

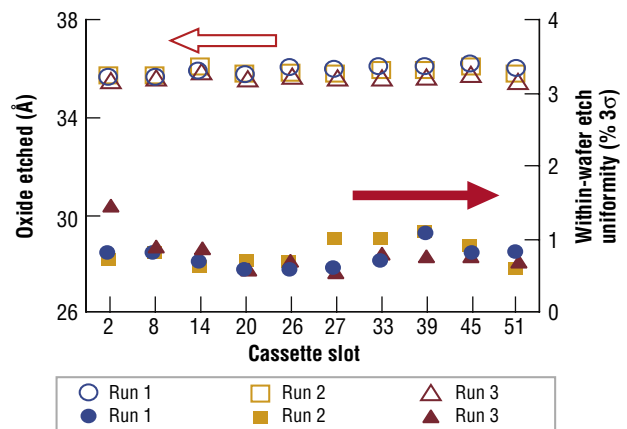


Figure 3. Thin-oxide etching results for SC1 (1:4:20, 10 min) in a separate quartz tank followed by DHF (200:1, 193 sec) in the STG rinser/dryer. The sample size was three runs with 10 oxide-etch monitor wafers in each run. An average of 35.9Å of oxide was removed. The average within-wafer uniformity was 0.8%, 3σ; wafer-to-wafer uniformity was 0.7%, 3σ; and run-to-run repeatability was 0.85%, 3σ.

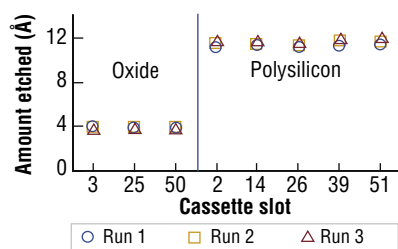


Figure 4. Thin-oxide and polysilicon etching results for SC1 (1:4:20, 10 min). The sample size was three runs with three oxide- and five polysilicon-etch monitor wafers in each run. An average of 4.0Å of oxide was removed with 0.2 range (max-min). An average of 11.5Å of polysilicon was removed with 0.9 range (max-min).

Once in the mixing manifold, the chemicals are dispensed into the tank through arrays of small holes located at the bottom of the tank. Because of its flexibility, the system can be used to generate a wide range of chemical mixtures when needed. **Figure 4** shows good etch performance in the SC1 quartz tank for oxide and polysilicon wafers.

Thin chemical oxide control for high-*k* preclean

It has been reported that depositing high-*k* materials directly on bare silicon has been problematic, leading to nonuniform nucleation, silicide formation, and decreased electron mobility. A solution to this problem is to leave the surface oxide-terminated prior to high-*k* deposition. An oxide-termination layer that is too thick will defeat the purpose of depositing a high-*k* material, however, so it is important to produce a very thin and uniform oxide-termination layer. The process to achieve a uniform, yet ultrathin, oxide layer on the silicon surface combines highly uniform saturated oxide growth using ozonated water with highly uniform oxide etching using in situ DHF injection, as previously

described [5].

After initially removing any native oxide in 200:1 DHF, the wafers are rinsed and then exposed to 30ppm ozonated water at room temperature. Exposure to ozonated water is held for 7 min to ensure optimal uniformity of the saturated oxide film. After rinsing away the ozonated water, the wafers are exposed to DHF using the well mixed chemical injection system for the required length of time to reach the desired final oxide thickness. **Figure 5** shows results of

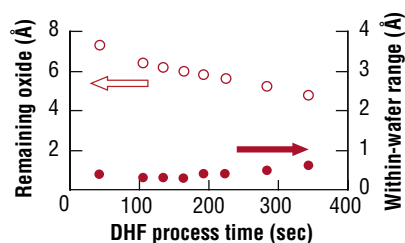


Figure 5. Thin-chemical oxide uniformity as a function of DHF process time.

the thin chemical-oxide uniformity as a function of DHF process time. Final oxide thickness down to 4.8Å was achieved with an across-wafer thickness range of 0.6Å. **Figure 6** shows the repeatability of this thin chemical oxide over the course of three runs.

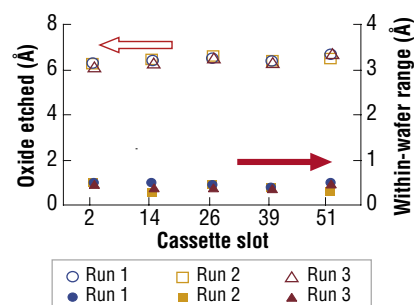


Figure 6. Thin-chemical oxide control. The sample size was three runs with five bare silicon monitor wafers in each run. An average of 6.5Å of thin oxide was controlled with 0.4 range (max-min).

Conclusion

A fully automated and flexible immersion system has been evaluated in a 65nm pilot line, demonstrating that advances in batch cleaning technology and concepts are capable of meeting critical process criteria for 65nm production. During the evaluation the system performed well for particle performance, and especially for thin-layer etch control. ■

Acknowledgments

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