SEMICONDUCTOR Manufacturing Magazine

WAFER CLEANING: 45 NM NODE

Wafer Cleaning Techniques For Meeting the Challenges of Advanced Semiconductor Manufacturing

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ON DECEMBER 13, 2005, THE MOST RECENT version of International Technology Roadmap for Semiconductors (ITRS) was introduced during a public conference in Seoul, Korea. From the presentations regarding semiconductor design and manufacturing, it is certain that the future of semiconductor manufacturing will continue to present significant challenges for both front-end-of-line (FEOL) and back-end-of-line (BEOL) surface preparation and critical cleaning steps (see Figure 1). This article reviews some of the most pressing challenges facing end-users, process tool manufacturers and materials suppliers, challenges that must be addressed in order to meet the progression of the ITRS.

SELECTIVE WET ETCHING CHEMISTRY

Front-end-of-line (FEOL) includes clean steps extending from a starting wafer to the first metal contacts. In FEOL, two trends pose significant surface preparation challenges within the next few years: implementation of high-κ gate dielectrics with metal gate electrodes, and the use of a “multi-gate” device structure. In film removal, high-κ gate dielectrics and metal gate electrodes will require selective-etching wet chemistry for processing. The flexibility of process equipment designs will be critical to provide rapid testing of a broad range of chemistries, dilutions and sequences. Cross-contamination concerns also become critical with multiple materials as the roadmap approaches 45 nanometers, thus driving the need for additional cleaning sequences to manage the new materials and new structures (see Figure 2).

> To meet the challenges set forth in the ITRS, IC makers need to employ a variety of cleaning technologies that address the wide range of challenges. These advances should be applied across multiple cleaning technologies, such as immersion, spray and aerosol technologies.

DAMAGE-FREE PARTICLE REMOVAL

The use of multi-gate devices at the 35 nm technology node will present an extreme challenge for damage-free particle removal. Single crystal silicon structures as narrow as 20 nm and as tall as 60 nm patterned on an oxide surface will need to be effectively cleaned without material loss or damage. Process equipment manufacturers need to extend development efforts in this area to meet this challenge. In many cases, equipment manufacturers will pursue partnerships to study and develop cleaning approaches for these new devices.

A significant trend is developing in the surface conditioning market as cleaning experts encounter challenges with simultaneous introduction of new materials, shrinking feature sizes (creating more fragile structures) and the tightening constraints on material loss.

Historically, wet benches with megasonic energy have dominated FEOL surface cleaning. At the 250 nm node, megasonic energy could no longer be used in several FEOL cleaning steps because it damaged gate structures. However, high

cleaning efficiency was still achievable with a non-megasonic wet bench, because high material loss, up to 5 Å, was acceptable. At the 90 nm node, non-megasonic wet-bench processes are much less efficient because allowable material loss has decreased to 1 Å. For example, a non-megasonic wet bench has particle removal efficiencies of greater than 90 percent for material loss of 5 Å, but close to zero percent for material loss of 1 Å or less. These tightening constraints have driven efforts to improve megasonics technology for damage-free processing. It has also driven development efforts in batch spray technology to reduce material loss, and in aerosol cleaning technology to eliminate pattern damage (see Figure 3).

PARTICLE REMOVAL FOR PROCESS FLUIDS

The reduction of particle contamination in FEOL wet cleaning chemicals is critical to meeting the new ITRS requirements. To achieve the purity requirements and maintain high manufacturing yields, advanced filtration membranes are employed to remove the sub-micron particles from cleaning chemicals used in recirculation baths and spray process tools. These filters must offer high flow rates, low differential pressure and high chemical resistance while removing increasingly-smaller particles from the process fluid.

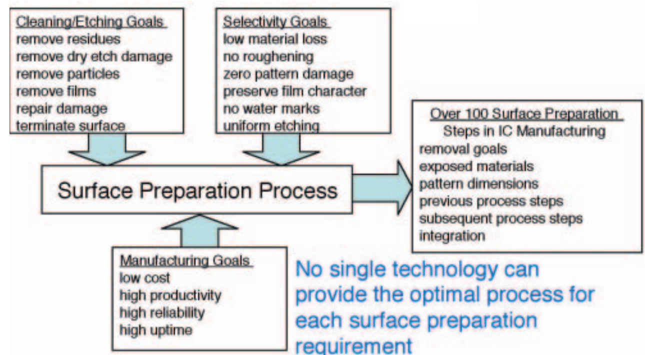
For the year 2007, the ITRS roadmap defines the "killer" critical particle size as 32 nm when the dynamic random access memory (DRAM) half-pitch is 65 nm. In 2010, when the DRAM half-pitch is 45 nm, the critical particle size is 23 nm. For particle removal of increasingly-smaller contaminants, advanced filtration technology for the 65 nm half-pitch must be ready and available today in preparation for the 45 nm half-pitch. Keeping filtration advances in pace with line-width reductions requires new production methods in membrane manufacturing and advances in polymer science to create application-specific modifications (see Figure 4).

MINIMIZED MATERIAL LOSSES

Over the past few years, a large portion of research and development into cleaning processes has focused on achieving high-efficiency particle removal while minimizing damage and material loss. Table 68 in the FEP chapter of the *2005 ITRS* defines the material-loss goals of this effort. Material-loss goals are defined for individual cleaning steps at each technology generation, and provide a 0.5 Å allowance for the 65 nm generation and a 0.3 Å allowance for the 45 nm generation.

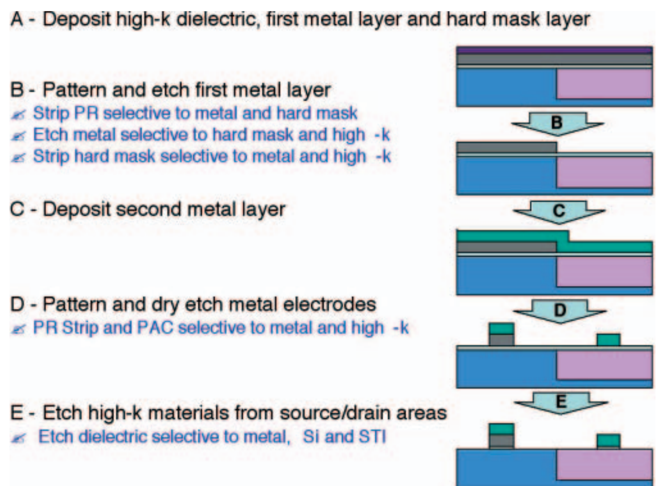
While development efforts have focused mainly on meeting these numbers and maximizing particle removal, the real goal of IC manufacturers is an integrated process sequence that minimizes the amount of silicon lost in the source/drain regions next to the gate electrode. The amount of silicon removed in these regions depends not only on the cleaning process, but also on the ashing and implantation steps. Ashing and implantation cause surface damage and oxidation, which lead to higher material loss during the cleaning step. Based on cross-sections published at the 2005 ASMC meeting by Dick James of Chipworks Inc., the total source/drain silicon loss on completed 90 nm generation chips can be measured at 90 to 130 Å.

FIGURE 1



Only through a variety of cleaning technologies will the broad spectrum of surface preparation challenges be addressed.

FIGURE 2



An example of a dual work-function advanced gate process flow, requiring several wet-etch and cleaning steps.

WET PROCESSES TO REPLACE SELECT ASHING STEPS

An integrated approach to controlling material loss during the fabrication process (e.g. optimizing several steps together instead of individually) has a higher probability of maximizing overall cleaning efficiency and final yield while also minimizing material loss and physical damage. One integration solution currently under investigation uses a wet process to achieve the complete removal of implanted photoresist, thus eliminating the ashing step (see Figure 5).

To strip highly-implanted photoresist, improvements have been made to the sulfuric acid – hydrogen peroxide process (also known as “piranha” or “Caro’s”) that allows for the elimination of the ashing step on most implant masks and results in a much lower overall silicon loss. This improvement is also driving advances in filtration technology, requiring filters to operate under higher residue-loading conditions and higher temperatures. Difficulties arise when the operating requirements call for efficient filtration with extended time between filter changes. Ultimately, new filter construction and membrane advances are needed to meet these challenges.

Understanding and optimizing the complete resist removal process sequence can result in better overall performance as well as lower cost and lower cycle time. In one analysis, the overall resist strip/clean cycle time could be reduced from 80 minutes to 45 minutes, reducing the typical 1.2 day-per-mask-level manufacturing cycle time by two to three percent. Tool manufacturers and component suppliers will continue to use the complete resist removal process to address other IC manufacturing challenges, such as environment, health and safety (EHS) concerns.

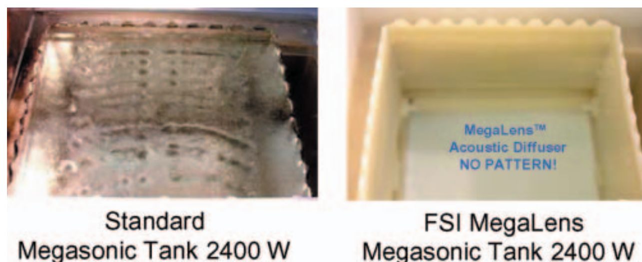
In BEOL, porous low-κ dielectrics will present challenges due to their chemical as well as physical structures. Standard photoresist ashing processes can cause damage to low-κ materials, so new methods must be discovered to prevent or repair this damage. Processes have been developed to silylate the low-κ material to replace organic groups that are lost during etching and ashing. In addition, progress is being made in developing all-wet photoresist stripping processes, which will prevent ashing damage to low-κ materials from occurring in the first place.

METAL ION REMOVAL AND PURIFICATION

The new materials proposed for the gate stack will require new processes and new methods for maintaining chemical purity during critical pre-cleans. Tables 115a and 115b in the ITRS yield enhancement chapter list the contamination levels for several process chemicals and ultra-pure water. As indicated in the notes for these tables, an effective method for minimizing the ionic contamination is to purify the incoming process chemical or deionized water with additional ion exchange. This removes ions by binding the contaminants to complexing agents immobilized on advanced ion exchange membrane cartridges, called purifiers.

Process chemical purification is gaining use in dilute chemical, DI water, hot DI water and organic solvent applications. For example, at the 45 nm DRAM half-pitch generation, IPA (isopropyl alcohol) used for Marangoni drying applications will likely require purification to remove ions and prevent deposits or water marks. For DI rinse steps, purification at the point of dispense will prevent metallic recontamination on the wafer surface.

FIGURE 3



The FSI MegaLens Acoutsic Diffuser significantly improves energy uniformity to allow damage-free cleaning.

FIGURE 4

Typical filter installation within a process tool.

CLEANING TECHNOLOGY TRENDS

At this time, there is no one cleaning technology for non-damaging, low-etch particle removal. Wet bench technology is focusing on improving megasonic energy fields and controlling dissolved gases to eliminate hot spots, and reducing material loss by using dilute chemicals. Centrifugal batch spray systems have successfully demonstrated higher particle removal efficiencies compared to non-megasonic wet benches due to greater hydrodynamic forces. Single-wafer spray technology has had success incorporating high-velocity spray jets, but has experienced limited adoption. Cryogenic aerosol tools have had excellent success in high-volume manufacturing for removing fall-on defects with a non-damaging, zero etch process.

To meet the challenges set forth in the ITRS, IC makers need to employ a variety of cleaning technologies that address

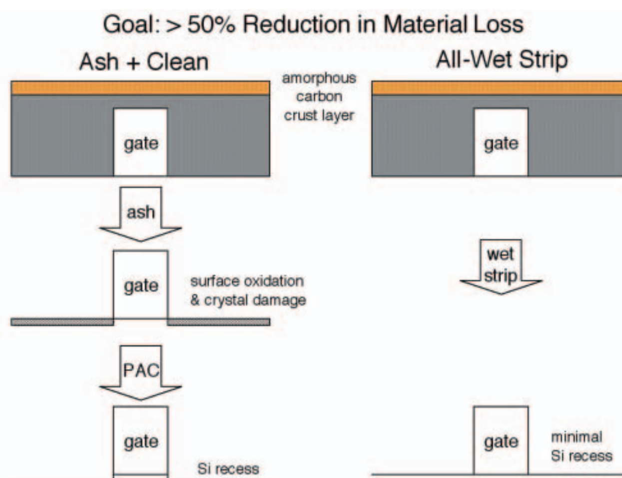
the wide range of challenges. These advances should be applied across multiple cleaning technologies, such as immersion, spray and aerosol technologies. Each technology will be supported by continued advances in filtration, purification and fluid delivery components to ensure optimal solutions are indeed ready to meet the rapid pace defined by the ITRS. For more information on ITRS current requirements and future developments, visit http://public.itrs.net.

The use of multi-gate devices at the 35 nm technology node will present an extreme challenge for damage-free particle removal.

As the director for the Entegris wet-etch, clean and plating markets, Charles Gould is responsible for creating and implementing market strategy. He graduated from the University of Minnesota with a B.S. in chemical engineering and a M.S. in the management of technology, and has over 10 years experience in semiconductor manufacturing.

Dr. Jeffery W. Butterbaugh is chief technologist for FSI International. He joined FSI in 1993 to lead process development for photochemical wafer cleaning. From 1995 to 2001, he was an engineering manager and led process development teams for anhydrous HF, cryogenic aerosol and immersion processing, as well as spray acid processing. Prior to joining FSI, he worked as a photolithography process engineer and a plasma etch development engineer for IBM in Burlington, Vermont and also as a sputter deposition and sputter etch engineer for Seagate Technology in Bloomington, Minnesota. He is currently serving as co-chair of the FEP Technology Working Group for the ITRS. Dr. Butterbaugh received his Ph.D. in chemical engineering from MIT and his B.S. in chemical engineering from the University of Minnesota. He holds eight U.S. patents and has authored or co-authored over 40 papers on surface conditioning and plasma etching.

FIGURE 5



The goal of all-wet resist stripping is to reduce material loss.

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