Advances on 45nm SiGe-Compatible NiPt Salicide Process

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Keywords: NiPt salicide, SPM, silicide, wet stripping, selective etching, HPM, SiGe

Introduction

NiPt self-aligned silicide (salicide) has become a major candidate for the 45nm node due to its better thermal stability and the surface morphology of NiSi on Si substrate [1,2]. SiGe has been proposed for PMOS strain engineering [3]. The relevant SiGe oxidation behavior [4], reaction with platinum [5] and thermal stress behavior [6] are important factors in developing a process for 45nm NiPt salicide over SiGe stressor. These concerns require the review of the current process for NiPt to verify its compatibility and extendibility.

The typical NiPt salicide process involves wet selective etching to remove unreacted NiPt by a hydrochloric acid (HCl) based aqueous solution. The HCl-based process has two platinum dissolution reaction scenarios [7]:

$$Pt + 4NO_3^- + 8H^+ \rightarrow Pt^{4+} + 4NO_2 + 4H_2O$$
$$Pt^{4+} + 6Cl^- + 2H^+ \rightarrow H_2PtCl_6 \qquad (1)$$

or

$$Pt + 2H_2O_2 + 4H^+ \rightarrow Pt^{4+} + 4H_2O$$
$$Pt^{4+} + 6Cl^- + 2H^+ \rightarrow H_2PtCl_6 \qquad (2)$$

However, using a chlorine-rich solution has raised concern about its suitability on silicide and SiGe due to its insufficient wet etch selectivity for 45nm processes. Therefore, a chlorine-free platinum dissolution and SiGe-friendly selective metal etching process is highly desired.

The dissolution of "finely divided" platinum in concentrated sulfuric acid under sufficiently high temperature has been reported [8]. The platinum dissolution scenario is as follows:

$$Pt + 2H_2SO_4 + 2H_2O_2 \rightarrow PtO^{2+} + 2HSO_4^- + 3H_2O \qquad (3)$$

Nevertheless, the required reaction temperature environment is not available from traditional wet bench and single wafer wet (SWW) tools. Recently, the FSI International ZETA® System ViPR™ process has reported the capability of achieving temperatures as high as 200°C on the wafer surface with pre-heated SPM through point of use (POU) mixing with various ratios [9]. This capability has potential application for a chlorine-free, SPM-only, NiPt selective etch process. This study is focused on developing an SPM-only selective etching process for 45nm NiPt salicide with SiGe devices. Better physical and electrical performance than the traditional HCl-based etching process has been demonstrated.

Experimental

Pattern wafers were prepared through the 45nm logic production process. Inspections for Pt residue and salicide damage after different selective etching processes were conducted on KLA-Tencor and SEM defect inspection tools. A multi-point electrical measurement was made after the formation of the metal1 layer to verify electrical performance. The sheet resistance measurement was conducted on both polysilicon (poly) gate conductor and single-crystalline silicon active areas (AA). In the wet etch process tool, process chamber temperature was measured with a built-in thermocouple mounted in the chamber wall. A higher chemical reaction temperature of SPM can be explored through various chemical ratios in POU mixing.

Figure 1 shows the highest (T2) reaction temperature can be found at an optimized mixing ratio of sulfuric acid and hydrogen peroxide with fixed pre-mixing sulfuric acid temperature. On the other hand, a higher than T2 chemical reaction temperature of SPM (T3) can be further reached by increasing the pre-mixing sulfuric acid temperature. Table I indicates three different chemical reaction temperatures of fresh-dispense SPM, T3>T2>T1, which were prepared to check wet clean efficiency with different reaction time. A current HCl-based selective etching baseline is also included to make a physical and electrical performance comparison with HCl-free SPM-only processes.

Results and Discussion

Figure 2a shows a traditional HCl-based selective etching process with a narrow process window inducing silicide damage. Using a 25-minute SPM-only etching process at temperature T1 prevents silicide damage, but Pt residue can be found at specific areas, as shown in Figure 2b. However, by using the SPM-only etching process at the higher T2 process condition, silicide damage is prevented and the unreacted NiPt layer can be fully removed, as indicated in Figure 2c. These results demonstrate a critical chemical reaction temperature of SPM needs to be reached to effectively remove residual Pt. The sheet resistance comparison of the NiPt salicide between HCl-based and SPM-only T2 selective etching condition (two wafers for each condition) is shown in Figure 3. The SPM-only T2 selective metal etching process indicates lower and tighter sheet resistance distributions at N+/P+ AA and poly areas in comparison to HCl-based etching.

Table II indicates increasing SPM chemical reaction temperature can effectively reduce selective etch process time without leaving Pt residue. As compared with the traditional HCl-based process time (30 min.), the SPM-only T2 condition can reduce the process time by 33% (20 min.) while SPM-only at the higher T3 temperature condition can reduce the process time by 66% (10 min.). The sheet resistance comparison of the NiPt salicide between the SPM-only T2 and SPM-onlyT3 processes are shown in Figure 4. These sheet resistance measurement data indicate a higher SPM chemical reaction temperature is not only helpful to improve process throughput but also provides better uniformity and tighter sheet resistance distribution.

The high temperature SPM-only T2 process was used to verify the selective metal etching process performance on SiGe-strained PMOS transistors, as shown in Figure 5a. The preliminary results indicate no damage found on SiGe-embedded polysilicon gate area, as indicated in Figure 5b. Figure 6 demonstrates comparable or better sheet resistance and uniformity performance on P+ poly and AA between the HCl-based baseline and the SPM-only T2 process condition.

Summary

A high-temperature, fresh-dispense SPM-only process is reported and evaluated for the 45nm CMOS NiPt salicide process with SiGe structures. The SPM-only processes with higher chemical reaction temperature yield lower and tighter sheet resistance distributions and up to 66% process time reduction. This SPM-only selective metal etching process is also proven to be compatible with PMOS strained SiGe structures. The next step is to evaluate the process extendibility of the fresh-dispense SPM-only process for the 32nm technology node.

Acknowledgement

The author would like to thank Steven Wang, Luke Chang, and Jeffery Butterbaugh at FSI International for their facilitation of high temperature SPM experiments.

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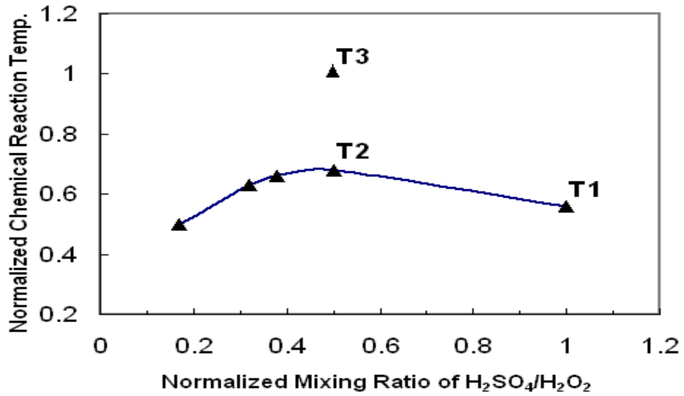

Figure 1: SPM chemical reaction temperature as a function of the mixing ratio of sulfuric acid and hydrogen peroxide.

Table I: Selective etch process test conditions.

Process Time	10 min.	20 min.	25min.	30min.	40min.
Baseline (HCl based)				V	V
SPM only - T1			V		
SPM only - T2		V	V		
SPM only - T3	V	V			

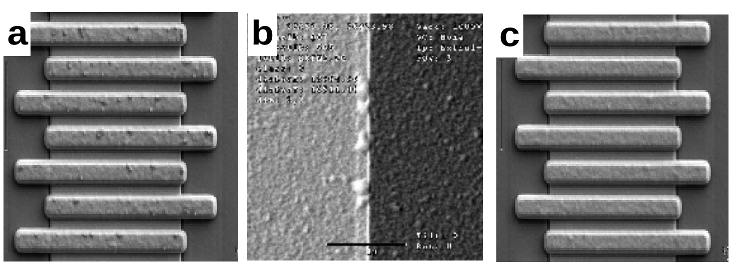

Figure 2: a) NiPt salicide damage by HCl-based 40min process time; b) Pt residue found at specific area for SPM-only T1 process; c) No salicide attack and Pt residue found for SPM-only T2.

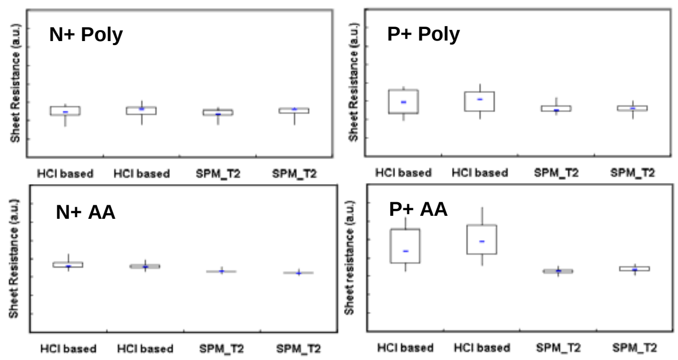

Figure 3: Sheet resistance comparison between HCl-based baseline and SPM-only T2 at N+/P+ AA and Poly areas.

Table II. Pt residue window as a function of etching process time

Process Time	5 min.	10 min.	15min.	20min.	25min.	30min.	40min.
Baseline(HCl based)	-	-	-	-	-	OK	NG
SPM only - T2	-	-	NG	OK	OK	-	-
SPM only - T3	NG	OK	OK	OK	-	-	-

NG: Pt residue or salicide damage; OK: No Pt residue and damage free

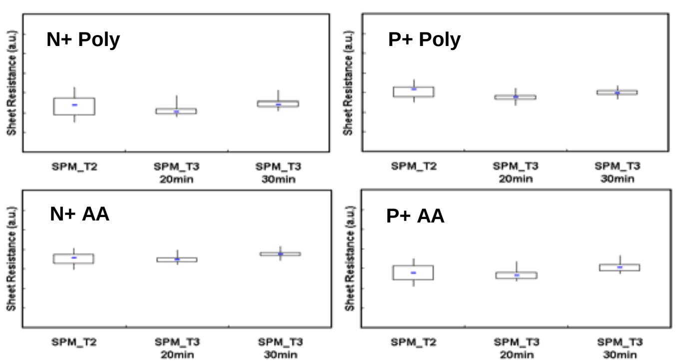

Figure 4: Sheet resistance comparison between SPM-only T2 and SPM-only T3 at N+/P+ AA and Poly areas

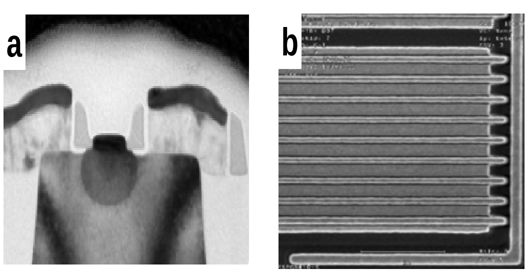

Figure 5: a) PMOS with SiGe structure; b) No salicide attack and Pt residue found for SPM-only T2 at SiGe areas.

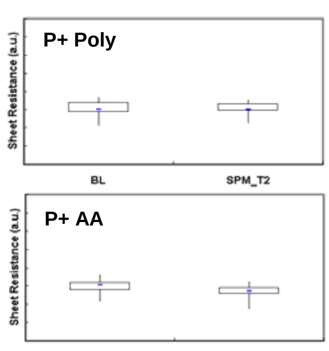

Figure 6: Sheet resistance comparison between HCl-based baseline and SPM-only T2 at N+/P+ AA and Poly areas.