

Front End Processes

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Scope

The Front End Processes (FEP) chapter of the ITRS (International Technology Roadmap for Semiconductors) focuses on future process requirements and potential solutions for the continued scaling of devices based on field effect transistors (FET); including high-performance, low-operating power and low-standby power logic devices; dynamic random access memory (DRAM) devices; and nonvolatile memory devices. This chapter defines comprehensive future requirements and potential solutions for the key front end wafer fabrication process technologies and materials associated with these devices. It addresses equipment and materials, as well as unit and integrated processes beginning with the substrate and extending through contact silicidation and deposition of strain layers. This chapter also addresses fabrication of storage nodes for the various memory devices.

The FEP chapter is divided into several subsections: starting materials, surface preparation, thermal/thin films, doping, plasma etch, DRAM, flash memory, phase-change memory and ferroelectric memory (FeRAM). Each subsection provides a forecast of scaling-driven technology requirements and potential solutions. As much as possible, the requirements tables are model-based, with the models described

in the table notes. The potential solutions figures serve to benchmark known examples of possible solutions, and are intended for researchers and interested parties.

They are not to be considered the only approaches. Indeed, innovative, novel solutions are sought, and their need is identified by red-colored regions of the requirements tables.

Materials-Limit Device Scaling

FET scaling has been the primary means by which the semiconductor industry has achieved the historically unprecedented gains in productivity and performance quantified by Moore's Law. These gains have traditionally been paced by the development of new lithography tools, masks, photoresist materials and critical dimension etch processes. In the past several years, it has become clear that despite advances in the ability to produce ever-smaller feature sizes, front end process technologies have not kept pace, and scaled device performance has been compromised. The traditional transistor and capacitor formation materials – silicon, silicon dioxide and polysilicon – have been pushed to fundamental material limits, and continued scaling has required the introduction of new materials. The current situation can be defined as “material-limited device scaling.” In addition, new approach-

es to device structure, such as nonplanar multi-gate devices, will be needed for future performance scaling.

Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures.

In no area is the issue of material-limited device scaling more clear or urgent than in the FET gate stack. Here, new gate dielectric materials having a higher dielectric constant than SiO_2 have been introduced to full production in 2008, along with metal in place of polysilicon for the gate electrode. Mobility enhancement and

channel-length scaling, which requires accelerated scaling of junctions to control short channel effects, will continue to provide enhanced device performance.

In addition, the end of planar bulk CMOS is becoming visible within the next several years. As a consequence, we must be prepared for the emergence of CMOS technology that uses nonconventional FETs or alternatives such as planar fully depleted SOI (FDSOI) devices and dual- or multi-gate devices, either in a planar or vertical geometry. The introduction of these devices will require the replacement of bulk silicon substrates with ultrathin, silicon-on-insulator (SOI) substrates and double- or multi-gate devices. The transition from extended bulk CMOS to nonclassical

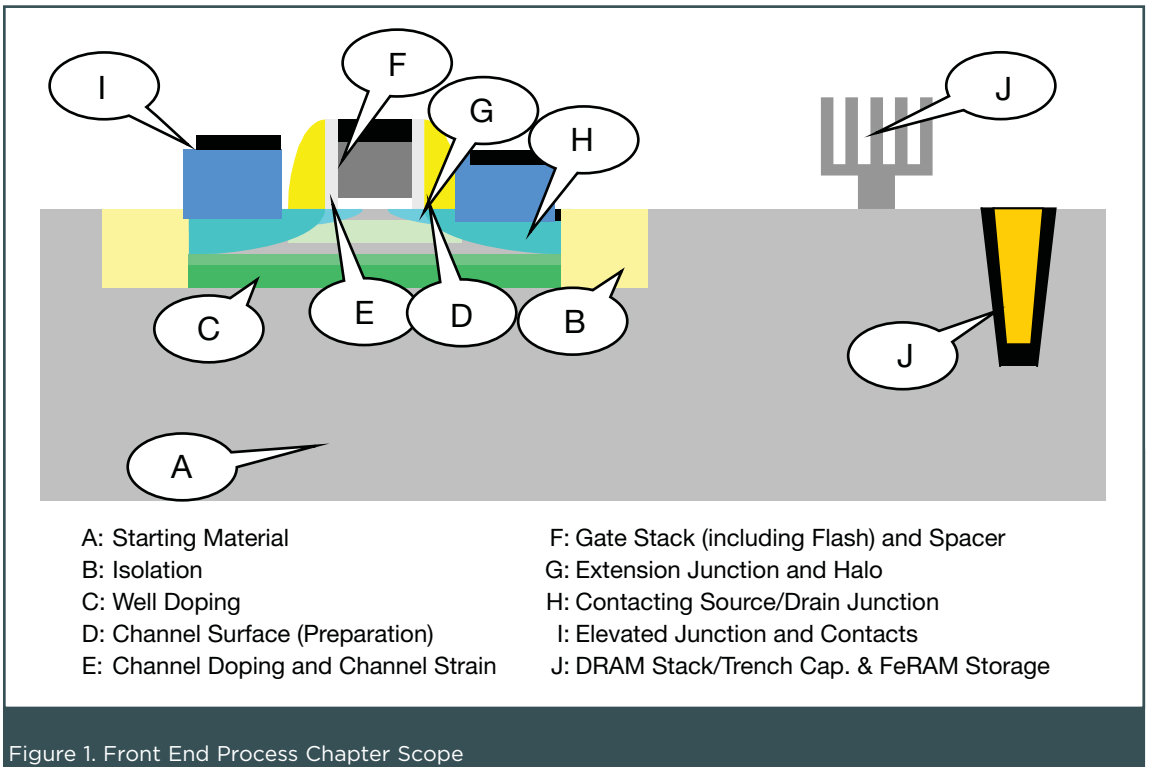


Figure 1. Front End Process Chapter Scope

device structures is not expected to take place at the same time for all applications and all chip manufacturers. Instead, a scenario is envisioned where a greater diversity of technologies are competitively used at the same point in time – some manufacturers choosing to make the transition to nonclassical devices earlier, while others emphasize extensions of bulk technology. This is reflected in the Thermal/Thin Films/Doping and Etching Technology Requirements Table FEP4 by the projection of requirements for multiple approaches in the transition years from 2010 through 2015.

of non-CMOS content, continue to find more applications within the industry. Also, higher productivity 300 mm fab approaches are being pursued. These trends may delay the need for 450mm wafers. The ITRS is actively considering how such approaches will impact overall productivity requirements. Should it be necessary to adopt the next diameter silicon wafer, there are concerns whether the incumbent techniques for wafer preparation can be cost-effectively scaled to the next generation.

Front end cleaning processes will continue to be impacted by the introduction of new front end materials such as high-κ

In starting materials, the projection of a 450 mm silicon substrate in 2012 is identified as a difficult challenge.

In the memory area, high-κ materials are now in use for DRAM capacitors. DRAM stacked capacitors are also now using metal-insulator-metal (MIM) structures. It is expected that high-κ materials will be required for the floating gate Flash memory interpoly dielectric by 2010, and for tunnel dielectric by 2013. The introduction of these diverse materials into the manufacturing mainstream is viewed as important difficult challenges. In addition, phase-change memory (PCM) devices are expected to make a commercial appearance by 2010.

In starting materials, the projection of a 450 mm silicon substrate in 2012 is identified as a difficult challenge. Such a diameter move is indicated to maintain pace with historic productivity enhancements based on augmented transistor count performance enhancements. However, so-called “More than Moore” approaches, which leverage enhanced design and/or inclusion

dielectrics, metal gate electrodes and mobility-enhanced channel materials. Scaled devices are expected to become increasingly shallow, requiring that cleaning processes become completely benign in terms of substrate material removal and surface roughening. Scaled and new device structures will also become increasingly fragile, limiting the physical aggressiveness of the cleaning processes that may be employed. In addition, these new device structures will require precise cleaning and characterization of vertical surfaces. DRAM stacked and trench storage capacitor structures will show increasing aspect ratios, making sidewall contamination removal increasingly difficult. Also, there is a challenge for particle scanning technology to reliably detect particles smaller than 28nm on a wafer surface for characterization of killer defect density and to enable yield learning.

2008 Update Highlights

Most of the FEP tables have required updates for 2008. The most significant updates occurred in Tables FEP4a and FEP4b - Thermal/Thin Films/Doping/Etch. The changes in FEP4 are driven by the new ORTC model of physical gate length scaling for high performance (HP), low operating power (LOP) and low standby power (LSTP) logic devices. Ideally, the FEP and PIDS teams would have liked to completely rework all of the device scaling models, adjusting CV/I scaling and taking into account the projected implementation of new CMOS structures, such as fully depleted SOI (FDSOI) and multi-gate/

FinFET (MG). However, due to limited resources in this “update” year, the FEP and PIDS teams decided to use the calculated table metrics from the 2007 ITRS publication by shifting and interpolating columns, using the physical gate length as the interpolation scaling factor. For the years 2007 through 2009, table metrics from the 2005 ITRS publication are used. In some years (2007, 2012, 2013 and 2016 for HP) the new ORTC physical gate length matches that for an earlier year in the 2007 or 2005 publication (2005, 2009, 2010 and 2012, respectively, for HP). In those cases, the metrics in that column are simply shifted to the new year. In most

Difficult Challenges < 22nm	Summary of Issues
Starting Materials	FDSOI Si and buried oxide thickness control
	SOI defectivity
	Surface particles
Surface Preparation	Surface particles not measurable
	Ability to achieve clean surfaces while controlling material loss and surface damage
	Metrology of surfaces that may be horizontally or vertically oriented relative to the chip surface
	Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface
	Achievement and maintenance of structural, chemical and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface
Thermal/Thin Films/ Doping/Etch	Continued scaling of HP multi-gate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation
	Continued EOT scaling below 0.7nm with appropriate metal gates
	Gate CD Control
DRAM	Continued scaling of capacitor structures for both stacked and trench type as well as continued scaling of dielectric thickness
Non-volatile Memory	Floating gate Flash technology considered unscalable beyond 22nm – new Flash NVM technology will be required
	Continued scaling of phase change memory technology
	Continued scaling of FeRAM technology

Table 1. Front-End Processes Difficult Challenges <22nm – 2008 Update

other cases, the new physical gate length in a particular year falls between the values in the 2007 roadmap. In those cases, the metrics for the new column are calculated by interpolating the values in each row using the physical gate length as the interpolation factor. This method of shifting and interpolating is used for HP and LOP metrics, but not for LSTP metrics, since the change in LSTP physical gate length scaling is relatively minor. FEP and PIDS recognize that this is not a completely satisfactory approach to accommodating the new ORTC physical gate length roadmap. This approach produces some “artifacts” that are discussed below. Both FEP and PIDS are committed to a complete recalculation of table parameters in 2009.

One artifact of the 2008 update “shift/interpolate” approach is a push out of metrics for FDSOI and MG devices and an exten-

sion of metrics for bulk planar devices. For HP logic, bulk planar metrics, which previously ended in the year 2012, now end in the year 2016. Metrics for HP FDSOI, which previously ran from 2010 to 2015 now run from 2013 to 2019, and metrics for HP MG, which previously started in 2011, now start in 2015. Similarly, for LOP logic, bulk planar device metrics which previously ended in 2012 now end in 2013; LOP FDSOI metrics, which previously ran from 2011 to 2016, now run from 2013 to 2018; LOP MG metrics, which previously started in 2011, now start in 2015. LSTP metrics for FDSOI prior to 2013 and for MG prior to 2015 are deleted so that FDSOI and MG start in the same year for all devices. At this time, FEP and PIDS are not sure if these shifts accurately represent when bulk planar will no longer be used in leading-edge device manufacturing or when FDSOI or MG will first be implemented in full manufactur-

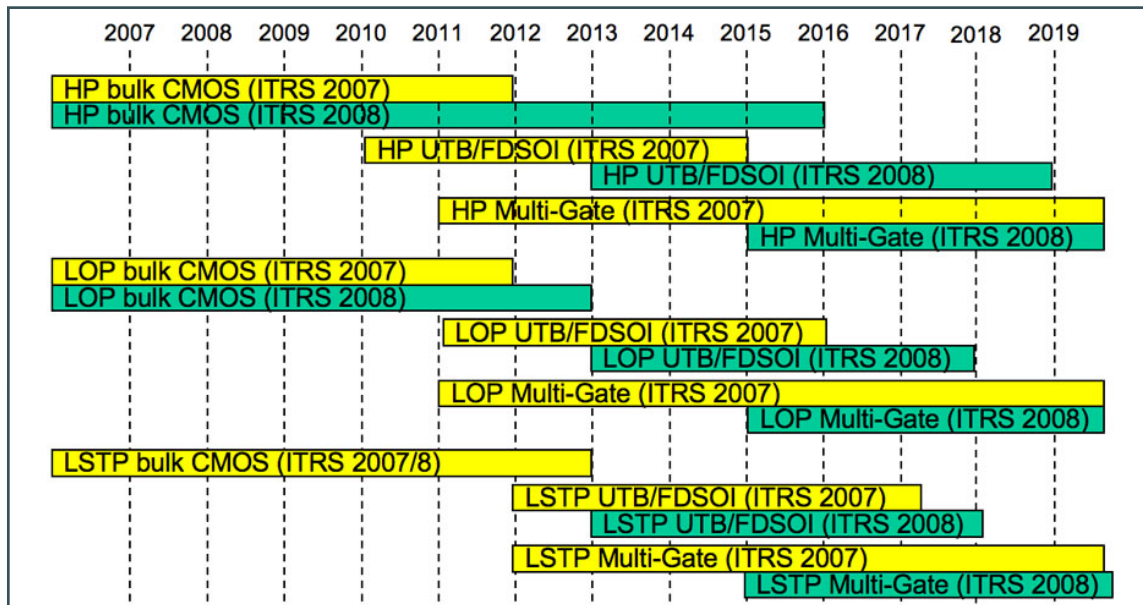


Figure 2. “Artificial” shift in expected introduction of FDSOI and MG structures due to “shift/interpolate” method used to accommodate the change in physical gate length scaling for the 2008 update. This will be fully reviewed and addressed in 2009.

ing. The timing of the implementation of these new device structures will be fully reviewed in the 2009 roadmap.

Another artifact is caused by using metrics from the 2005 publication. In 2005, some of the model assumptions were different, so some metrics from 2005 do not flow smoothly into the metrics published in 2007. In those cases, minor changes are made to smooth the transition. In addition, the six rows which are included in both the PIDS and FEP tables were compared and minor adjustments are made for complete consistency.

Updates are also made in the Starting Materials, Surface Preparation, Stacked DRAM, Trench DRAM tables. Most of these changes are related to a small change in the ORTC DRAM 1/2-pitch scaling for 2007-2009. For Trench DRAM, all table entries from 2009 through 2022 have been deleted, recognizing that the last developer of stand-alone trench DRAM devices announced the end of trench DRAM after the 58nm generation.

Summary

This article summarizes the 2008 Changes in the Front End Processes (FEP) chapter of the ITRS. This document focuses on future process requirements and potential solutions for the continued scaling of devices based on field effect transistors (FET), including high-performance, low-operating power and low-standby power logic devices, dynamic random access memory (DRAM) devices, and nonvolatile memory devices.

The current scaling situation is termed "material-limited device scaling." Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures.

In no area is the issue of material-limited device scaling more clear or urgent than in the FET gate stack. Here, new gate dielectric materials having a higher dielectric constant than SiO_2 have been intro-

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Updates were also made in the Flash and PCM Tables (FEP7 and FEP8). Information from Flash manufacturers show that the oxy-nitride-based technology can survive until 28nm for NAND and until 32-40nm for NOR with a transition period. Also, selective trench fill technology should overcome the intrinsic limitations of spin-on-dielectric. In FEP8, heater resistivity change is made less aggressive in consideration of the parallel increase of the reset current density.

duced to full production in 2008, along with metal in place of polysilicon for the gate electrode.

In addition, new approaches to device structure, such as nonplanar multi-gate devices, will be needed for future performance scaling. The end of planar bulk CMOS is becoming visible within the next several years. As a consequence, we must be prepared for the emergence of CMOS technology that uses nonconventional FETs or alternatives such as planar fully depleted

SOI (FDSOI) devices and dual- or multi-gate devices, either in a planar or vertical geometry.

Each Technical Working Group assembled a list of their most difficult challenges. This table is included in this document for your review. We would like to call attention to several of these, as they clearly are challenges that will shape the future of the industry in years to come.

The most significant updates occurred in Tables FEP4a and FEP4b - Thermal/Thin Films/Doping/Etch. The changes in FEP4 are driven by the new ORTC model of physical gate length scaling for high performance (HP), low operating power (LOP) and low standby power (LSTP) logic devices. These changes in device scaling timing resonate throughout the ITRS, and 2009 will have a focused effort to produce consistency in our tables.

In starting materials, the projection of a 450 mm silicon substrate in 2012 is identified as a difficult challenge. Front end cleaning processes will continue to be impacted by the introduction of new front-end materials such as high- κ dielectrics, metal gate electrodes and mobility-enhanced channel materials.

In the memory area, high- κ materials are now in use for DRAM capacitors. DRAM stacked capacitors are also now using metal-insulator-metal (MIM) structures. It is expected that high- κ materials will be required for the floating gate Flash memory interpoly dielectric by 2010, and for tunnel dielectric by 2013.

These are all truly critical issues facing the future development pathway of our industry. We have a clear vision of changes that need to be accommodated in the 2009 update of the roadmap, and we look forward to the challenge of facing these critical issues.

About the Authors

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Jeffery W. Butterbaugh is chief technologist for FSI International. He joined FSI in 1993. Prior to FSI, Dr. Butterbaugh worked for IBM and for Seagate Technology. He received his Ph.D. in chemical engineering from MIT and his B.S. from the University of Minnesota. He holds nine U.S. patents and is an author/co-author of more than 50 publications/presentations.

Larry Larson

Larry Larson joined SEMATECH in 1990, and currently coordinates the ITRS participation for the Front End Processes division in addition to coordinating academic efforts. He simultaneously has served as a professor in various roles at Texas State University at San Marcos since 2001. Dr. Larson received his Ph.D. in physics from Washington State University. He is an author/co-author of more than 120 publications/presentations.

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Raj Jammy is vice president of Materials and Emerging Technologies at SEMATECH. Previously on assignment from IBM, he has joined the SEMATECH staff and will continue to direct SEMATECH's Front End Processes division as well as lead efforts to tap in to emerging technologies with disruptive scaling potential. Jammy holds a doctoral degree in electrical engineering from Northwestern University. He holds more than 50 patents and is an author/co-author of over 170 publications/presentations. ■