

Resist Removal and Cleaning for TANOS Metal Gate Nonvolatile Memories

Enrico Bellandi, Cinzia De Marco - Numonyx (Italy)
Antonio Truscello, Jeffery W. Butterbaugh - FSI International, Minnesota



Abstract

Advanced nonvolatile memory devices utilizing metal gate stacks are not compatible with standard plasma ashing and wet chemical processes for resist removal and cleaning. These standard processes cause metal oxidation and metal etching, which damage the device. A new wet chemical approach for resist removal and cleaning has been developed using hot, 150°C, H₂SO₄ with very low levels of H₂O₂ followed by diluted NH₄OH.

Introduction

Charge trapping memory cells used in next-generation Flash memory architectures may require a structure with high-κ dielectrics as a blocking layer and a metal gate. In TANOS (tantalum nitride, alumina, silicon nitride, silicon dioxide, silicon) charge-trapping memory architecture, the polysilicon/silicide gate is replaced by a metal stack, while the polysilicon floating gate is replaced by a thin nitride layer, which acts as a charge trapping layer. A high dielectric constant (κ) layer, such as Al₂O₃, is used as the blocking layer (Figure 1).[1] TaN and W are often chosen as metal gate materials for their low resistivity, high

work function and compatibility with high-κ dielectrics.[2] An interlayer of WN can be used to promote the adhesion of the W on the TaN.

Standard photo-resist removal sequences, such as plasma ashing followed by wet treatments containing H₂O₂ or all-

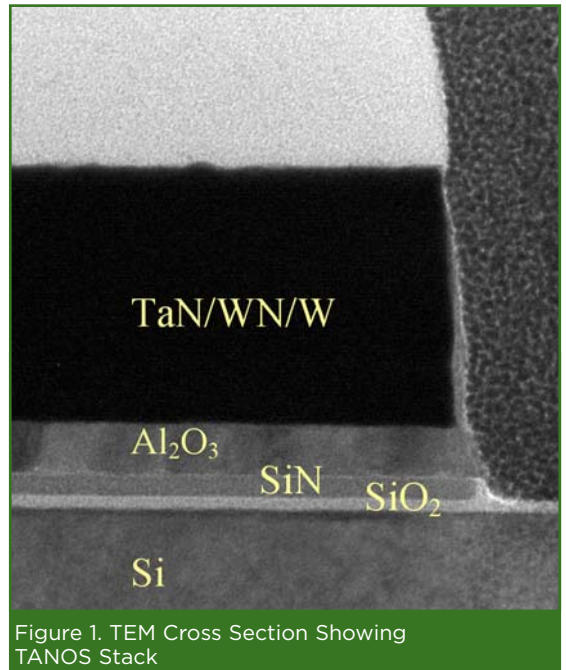


Figure 1. TEM Cross Section Showing TANOS Stack

wet treatments containing H_2O_2 , are no longer compatible with the materials used for the metal gate formation. O_2 plasma ashing can cause excessive oxidation of TaN, W and WN, while W and WN have a very high etch rate in many chemistries containing H_2O_2 , such as the $\text{H}_2\text{SO}_4 - \text{H}_2\text{O}_2$ mixture (SPM) or the $\text{NH}_4\text{OH} - \text{H}_2\text{O}_2$ mixture (APM), which is also known as “standard clean 1” (SC1). Solvents or proprietary products similar to the ones currently used for interconnection layers will introduce cross-contamination issues and are far more expensive than the conventional front-end inorganic chemistries.

Therefore, we evaluated alternative resist removal sequences, based on H_2SO_4 , NH_4OH and diluted HF acid, with little or no H_2O_2 . In this paper, we study the impact of resist removal sequences, including plasma ashing followed by inorganic

wet step and inorganic all-wet sequences, on TANOS metal gate materials (W, WN and TaN) and structures.

Experimental

Experiments were performed with 200 mm diameter silicon wafers. TaN was deposited in a PVD reactor, while W was deposited both in PVD and CVD reactors. Alumina was deposited in an ALD reactor.

O_2 and N_2/H_2 plasmas were produced by a microwave downstream reactor. The O_2 plasma was performed using two process times of 30s and 60s, while the N_2/H_2 plasma was performed using a single process time of 120s. A modified FSI ZETA[®] batch spray system was used for the wet treatments in the Numonyx facilities, while an FSI ZETA[®] system with ViPR[™] technology[3] was used for the experiments in the FSI facilities.

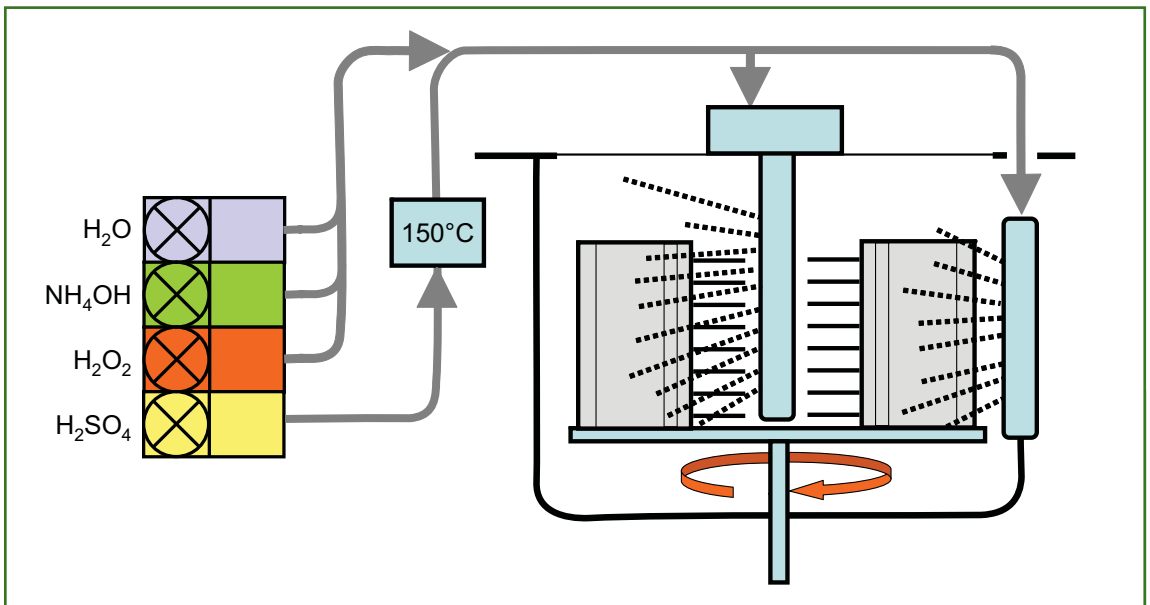


Figure 2. FSI ZETA[®] Batch Spray System With ViPR[™] Advanced Chemical Pre-Heater

A schematic diagram of the batch spray system is shown in Figure 2. Twenty-five 200 mm wafers are held horizontally in each of four process cassettes. The cassettes are placed on a turntable, which can be rotated at speeds up to 500 rpm in a nitrogen-purged chamber with a sealed lid. Chemicals, rinse water and nitrogen are dispensed from a central

gate devices. Metal contamination between products can affect the transistor characteristics or degrade the GOI.

According to A. Danel et al. [4], W, Ta and Ti are slow diffusers ($< 10^{-10}$ cm²/s at 950°C) that can precipitate at the silicon surface after a thermal treatment and are potentially harmful for the device reliability. Al is instead a slow diffuser that can affect

An important issue when introducing metals in front-end manufacturing is to avoid any form of cross contamination between front-end equipment.

spray post, which extends from the chamber lid, or from a side spray post mounted in the wall of the chamber. Up to eight different chemical streams can be mixed and diluted with hot or cold DI water using a mixing manifold. An in-line heater can be used to heat the chemicals before dispensing them into the chamber. The standard spray system is able to preheat chemicals to 95°C before dispensing. The ViPR™ hardware is able to preheat the chemicals to 150°C before dispensing.

Physical characterization of samples was performed by UV spectroscopic ellipsometry (KLA-Tencor FX200), XRF (PANalytical PW2830), AES (Nanoprobe PHI700), XPS (Physical Electronics 5700) and a Hitachi SEM.

Results and Discussion

Contamination Issues

An important issue when introducing metals in front-end manufacturing is to avoid any form of cross contamination between front-end equipment. The equipment used for high- κ metal gate processing is often used also for other levels or products with conventional polysilicon

the GOI. Danel et al. recommend a metal contamination level less than 10¹⁰ at/cm² (5x10¹⁰ at/cm² for Al) for pre-diffusion cleaning and less than 10¹¹ at/cm² for other FEOL cleaning steps. The contamination level after processing high- κ and metal gate materials was therefore verified before and after the removal and cleaning tests in the batch spray system. All measured metal levels were below the mentioned limits.

Influence of Dry Ashing

A possible issue for metal gate integration is metal oxidation caused by dry resist removal treatments. While O₂ plasma ashing is widely used in the front-end for bulk resist removal, N₂/H₂ plasma can be a suitable nonoxidizing alternative, even if it does not provide the same stripping efficiency. Auger analysis showed that the surfaces of TaN, WN and W layers are oxidized by O₂ plasma, while no surface oxygen increase was observed after an N₂/H₂ plasma treatment.[5]

XPS analysis on as-deposited samples detected a thin WO₃ oxide on W and WN, and a Ta₂O₅ oxide on TaN. The O signal

relative to these oxides significantly increases after O_2 plasma treatment. In the case of N_2/H_2 plasma treatment, the N signal increases at the surface, indicating the formation of a thin layer of N-rich metal.

UV extended spectroscopic ellipsometry was used to estimate the oxidized layer thickness. O_2 plasma treatment for only 30s can grow a 5-10nm thick oxide on the surfaces of the metals.

Wet Cleaning After Dry Ashing

In conventional front-end processing, resist removal is usually accomplished with

a two-step process composed of a first plasma ashing step and a second wet chemical cleaning step. We have studied the influence of the plasma ashing step on the metal etch rate during the wet chemical cleaning step. Thickness measurements before and after wet cleaning showed that the presence of the surface oxide created during the ashing step increases the wet etching amount from 1-2nm on the as-deposited sample to 4nm on the O_2 plasma-treated tungsten. Such a large etch is not compatible with the sub-32nm memory cell critical dimension (CD) requirements.

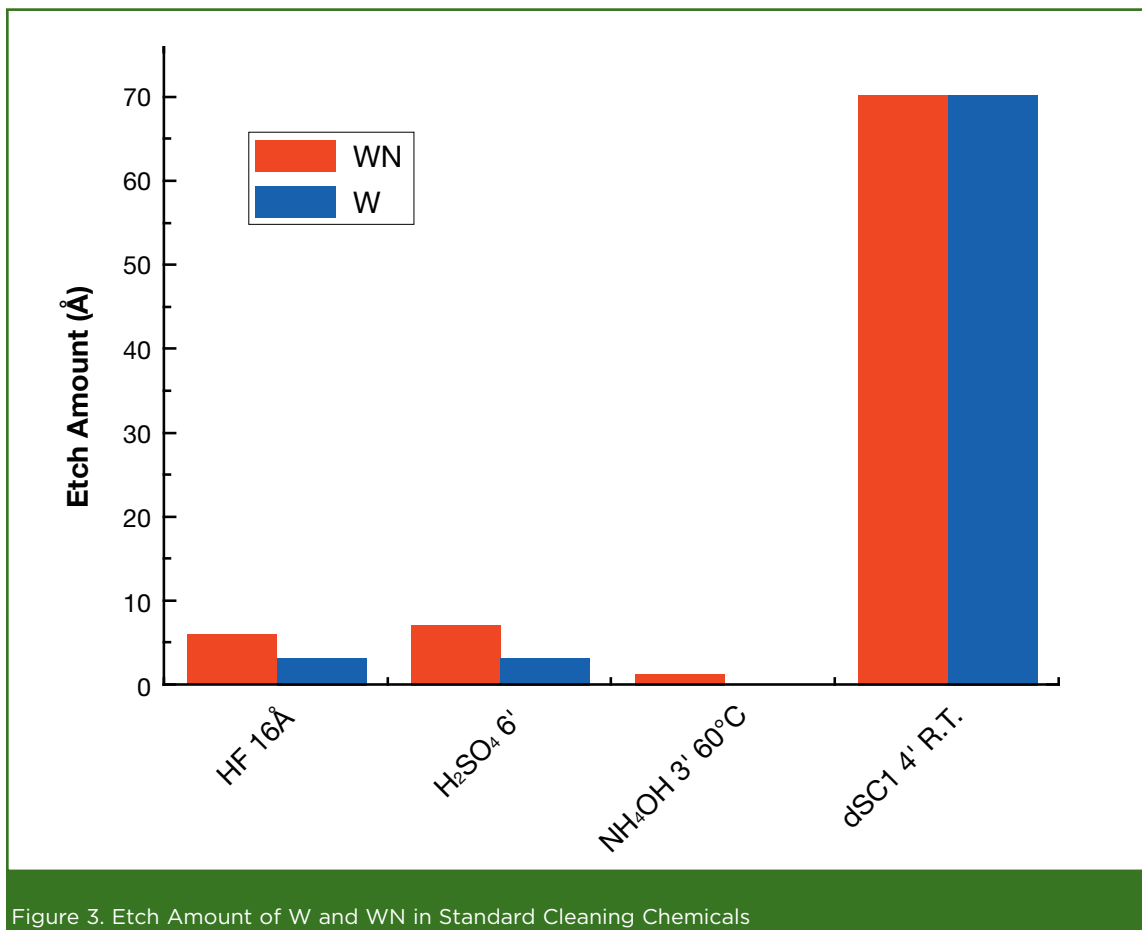


Figure 3. Etch Amount of W and WN in Standard Cleaning Chemicals

Therefore, the oxygen ashing treatment should be avoided when using TaN or W metals in the gate structure.

Effect of Standard FEOL Chemistries on Metal Gate Stack

As a preliminary study, we verified the etch rate of each material in some commonly available chemicals and mixtures, such as HF, H₂SO₄, NH₄OH and SC1. Results for W and WN are reported in

Figure 3. SC1, even if performed at room temperature and with the highest dilution possible on our equipment, showed a very high etch rate, while H₂SO₄ and HF, as well as diluted NH₄OH, showed good material compatibility. Conventional SPM is well known to rapidly etch these materials, and the etch rate in this study was too high to be correctly estimated. TaN and thermally treated Al₂O₃ are indeed compatible with most of the baseline chemistries, including

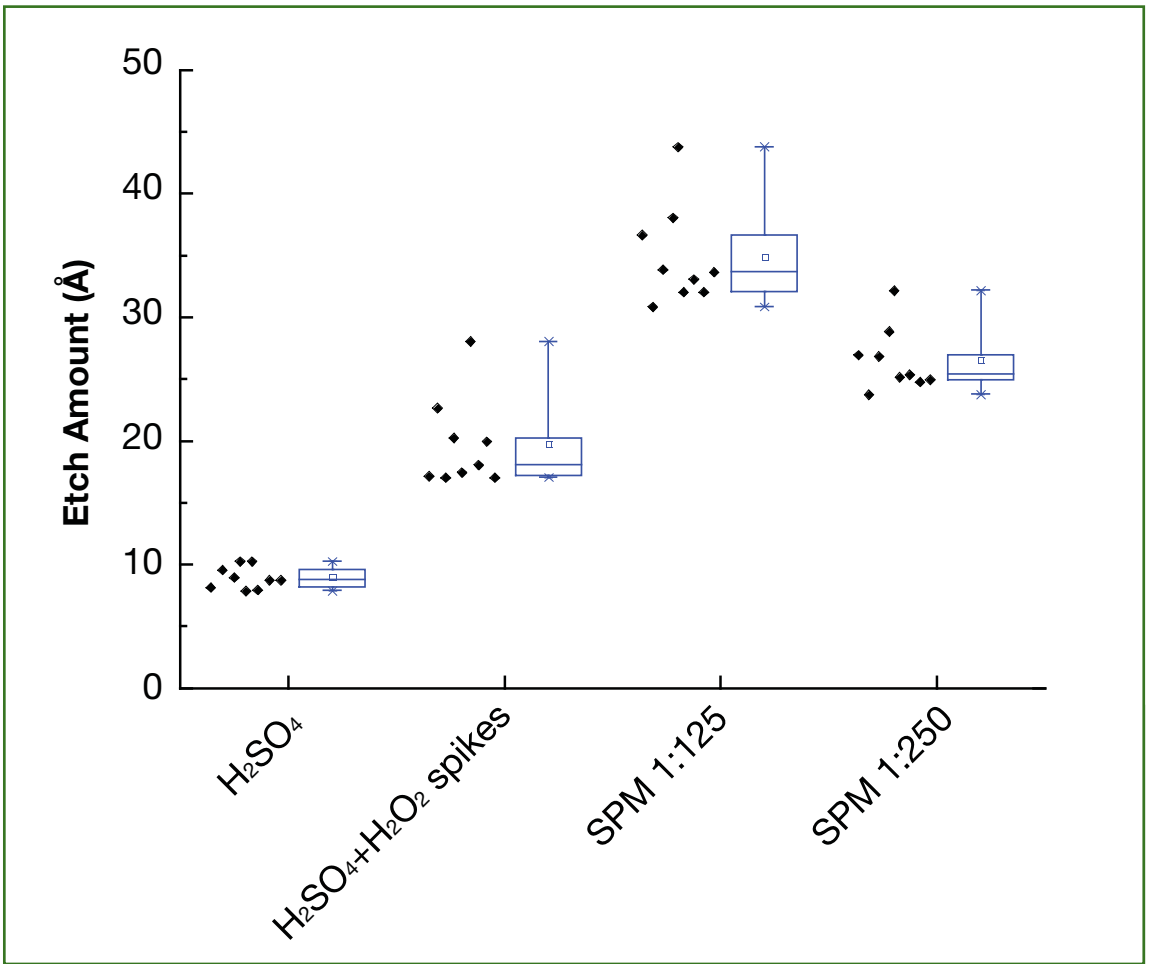


Figure 4. Etching of W metal with various 150°C H₂SO₄ mixtures. The chemical process time is 240 seconds in each case.

SPM and SC1. Therefore, we considered a simple resist removal sequence consisting of a hot H_2SO_4 step followed by a 40°C diluted NH_4OH step.

The H_2SO_4 - NH_4OH sequence etches less than 20\AA of WN and W, while the SiO_2 and TaN etch is less than 1\AA . Even though this treatment has a low impact on the gate CD, it cannot be applied when bare, HF-treated silicon or polysilicon are exposed (e.g., transistors) because NH_4OH attacks silicon, causing significant roughening. If a very low amount of H_2O_2 is mixed with H_2SO_4 , the silicon surface is chemically oxidized, preventing etching and roughening by NH_4OH . Adding H_2O_2 spikes to the H_2SO_4 step causes the W and WN etch rate to slightly increase, while the polysilicon etch decreases to very low values. Consequently, defectivity on bare silicon is drastically reduced. Moreover, the addition of H_2O_2 improves the removal efficiency of resist and organic anti-reflective coatings.

As described above, the ViPR™ hardware option provides much higher chemical temperature in the process chamber, reducing the amount of H_2O_2 required for resist removal. The amount of W etched using H_2SO_4 preheated to 150°C with various amounts of added H_2O_2 is shown in Figure 4. In order to achieve a low W etch at such high temperatures, it is required to keep the H_2O_2 concentration very low (1:>250 ratio) or to spike it, adding H_2O_2 only for short periods throughout the H_2SO_4 dispense time.

Resist removal and cleaning solutions on metal layers may lead to metal corrosion on some specific structures by chemical etchants such as H_2SO_4 . [6] The corrosion rate increases with increasing acid concentration and with increasing temper-

ature. In our experiments, during one process step we observed isolated metal gate structures lifted after the low H_2O_2 SPM/ NH_4OH wet resist removal process. Electrochemical corrosion could be enhanced by the different grounding of these structures with respect to the more densely packed structures. This problem can be resolved by adjusting the process flow of liner deposition and etching to avoid excessive exposure of the metal gate to the cleaning process.

Conclusions

Conventional O_2 plasma ashing resist removal sequences and standard wet cleaning chemistries, such as SC1 and SPM, cannot be applied to TANOS-like metal gate stacks because of metal oxidation by O_2 plasma and metal etching by H_2O_2 . Dry ashing treatments considerably modify metal surfaces, affecting their stoichiometry and wet etch rate. The O_2 plasma ashing process grows an oxide layer on the metal surface that can be etched in the following wet removal or cleaning steps. N_2/H_2 plasma is not compatible with the 32nm memory cell CD requirements.

A new wet chemical approach to resist removal and cleaning steps has been developed that is compatible with TANOS metal gate stacks. 150°C H_2SO_4 with very low levels of H_2O_2 spiking followed by diluted NH_4OH can be used for resist removal and cleaning applications and is now being used in integrated circuit manufacturing for multiple cleaning steps.

Acknowledgments

The authors would like to acknowledge A.C. Elbaz, E. Ravizza and L.M. Avaro for the in-line metrology and physical analysis, and F. Zanderigo for the process integration support.

References

1. C.-H. Lee, J. Choi, C. Kang, Y. Shin, J.-S. Lee, J. Sel, J. Sim, S. Jeon, B.-I. Choe, D. Bae, K. Park and K. Kim, 2006 Symposium on VLSI Technology, Digest of Technical Papers (2006) 21-22.
2. C.-H. Lee, K.I. Choi, M.K. Cho, Y.H. Song, K.C. Park and K. Kim, Electron Devices Meeting, 2003. IEDM 2003 Technical Digest, IEEE International (2003) 26.5.1-26.5.4.
3. K.K. Christenson, J.W. Butterbaugh, T.J. Wagener, N.P. Lee, B. Schwab, M. Fussy, and J. Diedrick, Ultra Clean Processing of Semiconductor Surfaces VIII, Solid State Phenomena 134, (2008) 109.
4. A. Danel, D. Renaud, P. Besson, C. Bigot, A. Grillouillet, J.P. Joly, M. CLaes, T. Bearda, J. Frickinger, ECS Transactions (2005) Vol. 1, No. 3.
5. A.C. Elbaz, E. Bellandi, C. De Marco, L.M. Avaro, E. Ravizza, R. Piva, Ultra Clean Processing of Semiconductor Surfaces IX, Solid State Phenomena 145-146, (2009) 257.
6. Karen Alves de Souza and Alain Robin, Materials Chemistry and Physics Vol. 103, Issues 2-3 (2007) 351-360. ■

About the Authors

Enrico Bellandi

Enrico Bellandi holds a physics degree from the University of Pavia, Italy. He worked at STMicroelectronics for 14 years

before joining Numonyx. He is now a wet processing expert in the Numonyx R&D Center in Agrate Brianza, Italy.

Cinzia De Marco

Cinzia De Marco holds a degree in material sciences from the University of Milano-Bicocca, Italy. She has worked at STMicroelectronics for three years before joining Numonyx. From 2005 to 2007, she was an assignee in the IMEC Ultra Cleaning Processing group.

Antonio Truscello

Antonio Truscello received an M.S. degree in mechanical engineering from the University of Catania, Italy. He joined FSI International in 2003, and is now a field applications manager in Europe. Previously, he worked for FSI's European distributor, Metron Technology, as an application engineer.

Jeffery W. Butterbaugh

Jeffery W. Butterbaugh is chief technologist for FSI International. He has also worked for IBM and Seagate Technology. Dr. Butterbaugh received his Ph.D. from MIT and his B.S. from the University of Minnesota. He holds nine patents and is author/co-author of over 50 publications/presentations.

[Click here to return to Contents Page](#)

